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E.g., add together these 100 pairs of numbers to produce 100 results

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This is called *single instruction multiple data* (SIMD) processing

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We can get both process and data parallelism from this architecture

The hardware is commodity, so clusters with thousands of CPUs are common; clusters with millions of cores exist

Background

Some words: be aware different people use these terms in different ways

- core: a single processing element, can be just an ALU or can have its own instruction decoding unit
- cpu: sometimes just a synonym for core, sometimes a chip which contains one or more cores
- processor: similar to cpu
- node: a motherboard that can have one or more slots for multi-core cpus that share some local resource on the motherboard, particularly memory
- cluster: a collection of nodes connected by a network

Background

For example, the Azure machine you will be using for the coursework has four nodes, each consisting of two chips, each with 24 cores

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From `www.top500.org`, the fastest (publicly known) computer in the world is (June 2023):

> Frontier (USA), 8,699,904 cores, comprising AMD EPYC 64C cpus at 2GHz; plus Radeon Instinct GPUs; using 23MW power; with Slingshot-11 interconnect; running HPE Cray OS

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1 exaflop is a quintillion (10^{18}) floating point operations per second

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HPE Cray OS is a variant of SUSE Linux Enterprise Server

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But lots of cores is easy: just expensive

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> *Anyone can build a fast CPU. The trick is to build a fast* **system***.*
> Seymour Cray

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Programming a cluster is all about moving the data: we might be able to do a million machine instructions in the time it takes to fetch some data from another node

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On a machine with a million cores it can be faster to do a million adds on one core rather than ship out the adds to the CPUs; do a million adds in parallel; then collect the data back together

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Just having an immensely parallel machine doesn't mean it's always better to use the parallelism

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A very different mindset is needed!

Classifications

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- Multiple Instruction, Multiple Data (MIMD). Multiple cores doing different things to different datastreams. What most people (wrongly) think parallel computing is all about

Classifications

- Multiple Instruction, Single Data (MISD). Something to fill in the last combination of letters. Sometimes interpreted as *redundancy*, e.g., airplane flight control where they have multiple (different!) computers all processing the same data

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		Data	
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Instruc-	Single	SISD	SIMD
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- Single Program, Multiple Data (SPMD). Recall SIMD runs the same program on multiple cores in *lockstep*, so every core is executing the same instruction. SPMD runs the same program (on different data) on a MIMD machine, with each core going their own way, particularly on loops and conditionals

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- Multiple Program Multiple Data (MPMD). A MIMD machine not running SPMD. So each core running potentially different programs, e.g., producer-consumer models, or systolic pipelines (see later)

Classifications

Of course, there are many more classifications we need to look at

Classifications

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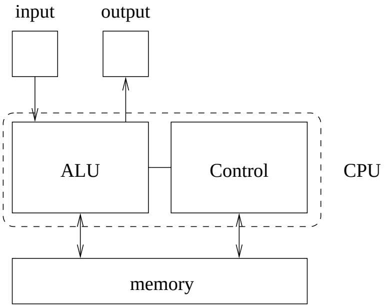
We can think of how the parts of the architecture are connected

Classifications

Uniprocessor

A *uniprocessor* (*unicore*) or *sequential processor* is the traditional von Neumann architecture of a single CPU, memory, etc.



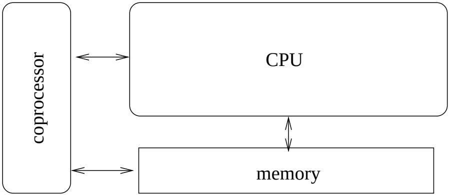
von Neumann Architecture

A hugely successful model that enabled the computer revolution to take place

Classifications

Coprocessor

A *coprocessor* is a non-general processor used as a worker by the processor



Coprocessor

Currently very popular in the form of graphics cards

Classifications

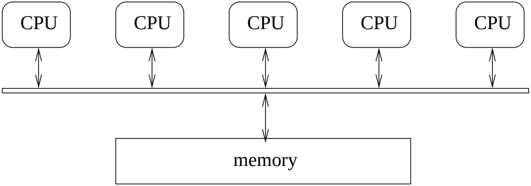
Multiprocessor

A *multiprocessor* is a loose term applying to most parallel architectures, except occasionally SIMD, which usually doesn't have multiple full cores

Classifications

Shared Memory

A multiprocessor has *shared memory* when the cores access memory on a shared bus



Shared Memory

Cores share each other’s data: if one core modifies the value of a value in memory, the other cores see that change

In reality, the shared bus can be a lot more complicated, e.g., a tree or ring structure

Classifications

Shared Memory

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In this example, we have *symmetric* shared memory: every CPU has the same equal access to the shared memory

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In particular, the memory is a bottleneck

Memory and memory buses are slow relative to a processor anyway, and when you have several cores all trying to access memory simultaneously it gets much worse

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Even single core processors have a problem with the speed disparity, so they use fast (but small) intermediate cache memory

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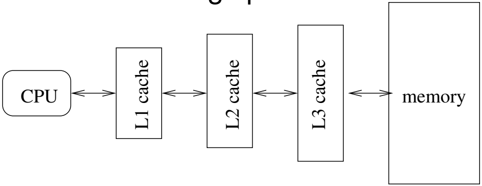
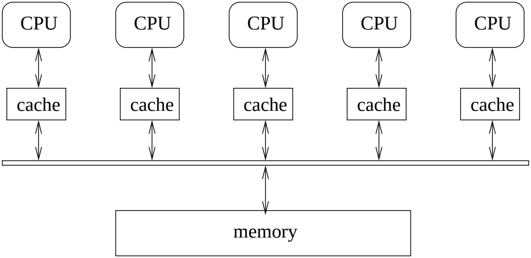


Levels of cache

Classifications

Shared Memory

So shared memory machines try to cut down the traffic on the bus by using caches



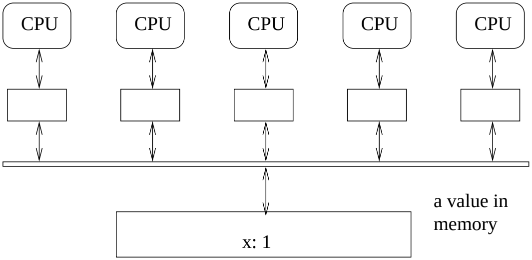
Memory caches

Each core has its own chunk of fast cache memory: this cuts down on use of the bus

Classifications

Shared Memory

If a core is manipulating the value of a variable it will be loaded into the cache and operated on there, rather than over the bus in main memory



A value in memory

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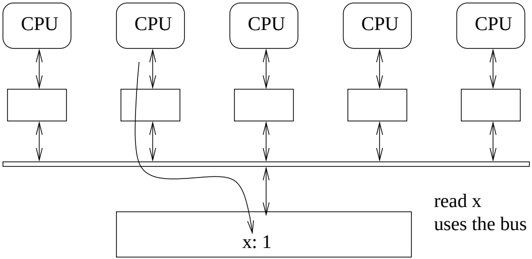

Read value

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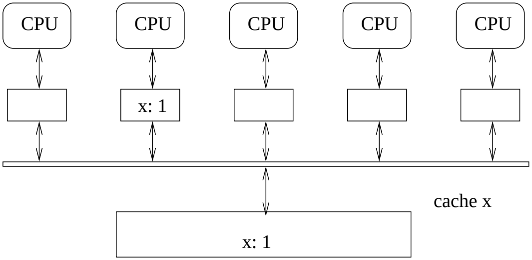

Copy in cache

Classifications

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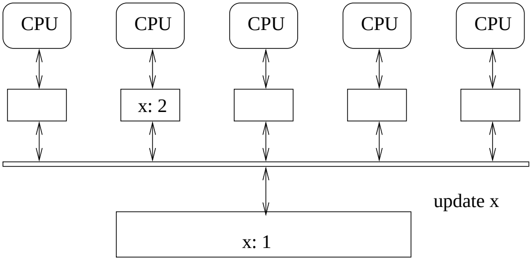

Update x (in cache)

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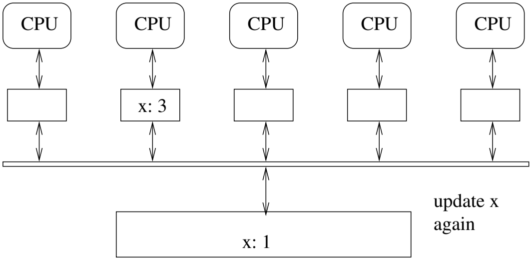

Update x again

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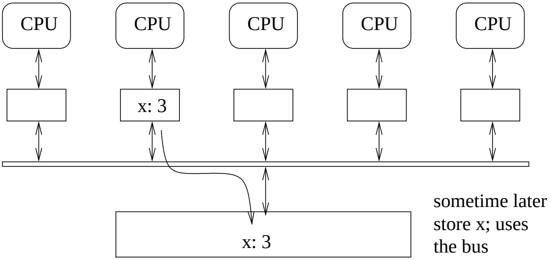

Store x later

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Shared Memory

This reduces pressure on the shared bus: but now we have the problem of *cache coherence*

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This reduces pressure on the shared bus: but now we have the problem of *cache coherence*

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So if another core want to read the value before the updated version has been written back, it will get the old value

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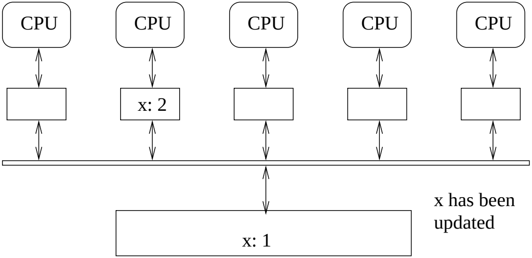
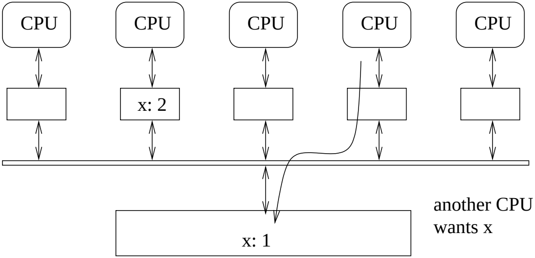
Shared Memory



x has been updated in cache

Classifications

Shared Memory



Another CPU wants x

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Even worse, dependent on timing, you don't know if the first CPU has written the value back or not

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This particular example is a *data race*: a race condition that involves updating data

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You might get the right answer on hundreds of runs; it doesn't mean your program is correct!

And it might always happen to be right on your machine, but wrong when run on some other machine

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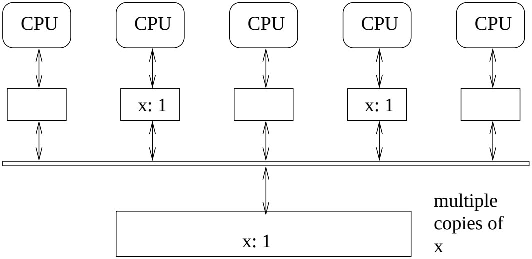
When one core updates the variable the other cores will still be using their own in their caches

Classifications

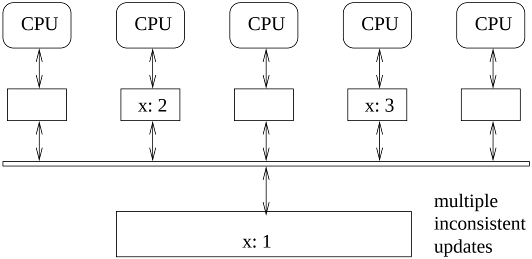
Shared Memory



Multiple copies of x

Classifications

Shared Memory



Multiple inconsistent copies

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E.g., in the *snarfing* protocol, whenever an update is made the value is immediately written through the bus (increasing traffic on the bus. . .) to main memory. The other caches are watching the bus and if they have a copy of the variable they update their copy with the value being written (they “snarf” the new value)

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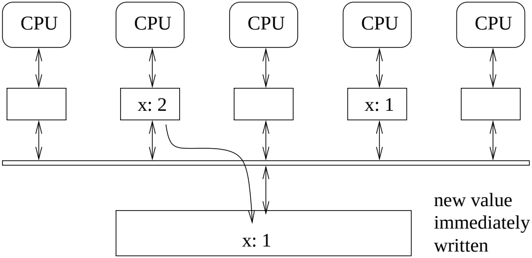
This is expensive in hardware and does not scale well to large number of cores as every write must go through the bus

Classifications

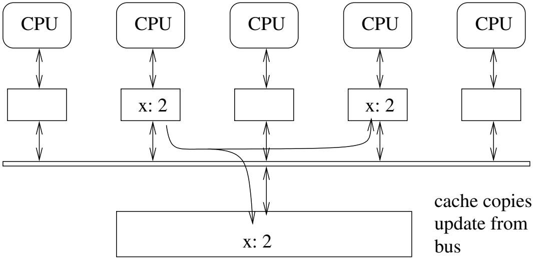
Shared Memory



New value immediately written to memory

Classifications

Shared Memory



Caches copy update from bus

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Shared Memory

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Secondly, well-written code will avoid using shared values in the first place. Sharing mutable state across threads is bad design (more on this later)

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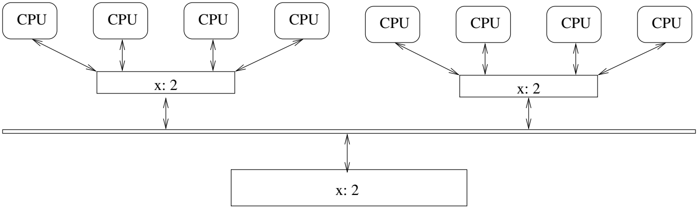
You could use very fast buses and main memory: not a solution due to cost

Or use slow processors: IBM tried this and it was surprisingly good!

Classifications

Shared Memory

Exercise Modern architectures are more like:



Modern memory architectures

Does this solve the problem?

Classifications

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Intel have just announced a 288 core x86 chip (Sept 2023)

Classifications

Shared Memory

Exercise Read about cache coherence mechanisms: snoopy caches; directory based; snarfing; MSI; MESI

Exercise Another complication to symmetric shared memory is when the *cores* are not identical: read about *performance* and *efficiency* cores (P-cores and E-cores) used by Intel, Apple and others