Classifications

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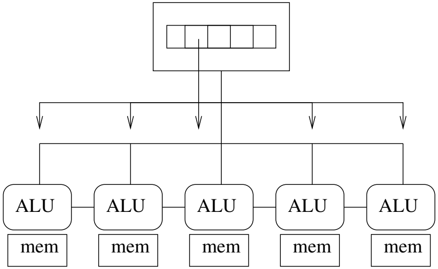
Sometimes called a *broadcast*

Classifications

Vectors

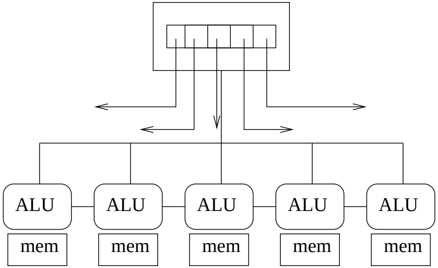


One read goes to all cores

Classifications

Vectors

However, as is often the case, it can be that each core wants a value from a different part of global memory. E.g., core *k* wants the *k*th element from a array



Reading a vector of values

Classifications

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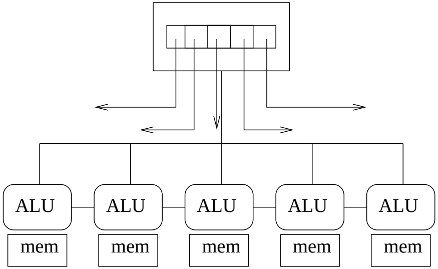
The next 16 values are sent in the next transfer; and so on

Classifications

Vectors



A single fat read goes to multiple cores

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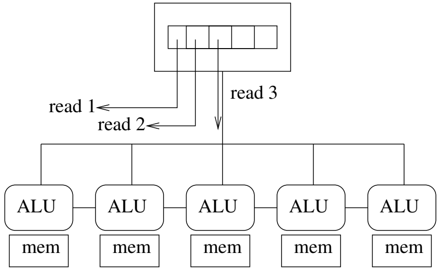
E.g., proc k wants value k^2 from the array

Classifications
Vectors



Awkward distribution done in multiple reads

Classifications

Vectors

Similarly for writes: e.g., core *k* writing a value to the *k*th slot in an array could be coalesced

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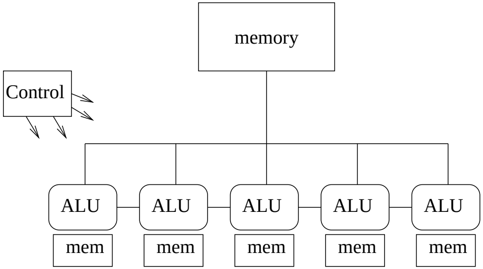
Exercise Consider the case of indirecting through a pointer to local memory (a) when it's pointing to the same location on all cores and (b) when it's pointing to a different location on each core

Classifications

Vectors

Often there is fast direct communications between neighbouring CPUs



Neighbour connections

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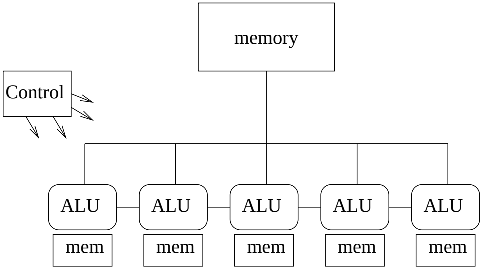

Neighbour connections

This allows data to shuffle up and down the vector very quickly: many problems (e.g., differential equations solving) work on data and neighbour data in this way

Classifications

Arrays

Clearly, vector processors are SIMD and not suitable for MIMD or even SPMD

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Vector processors appeared early in parallel computing as they are relatively easy to build: ALUs are relatively easy to build and replicate, while control units are complex and hard

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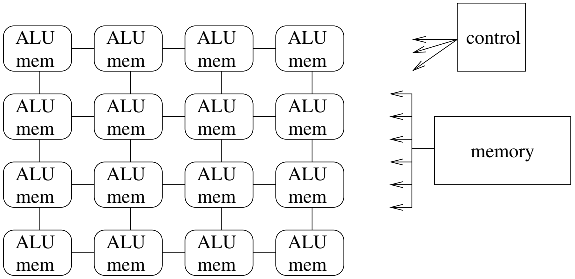

Array processor

Classifications
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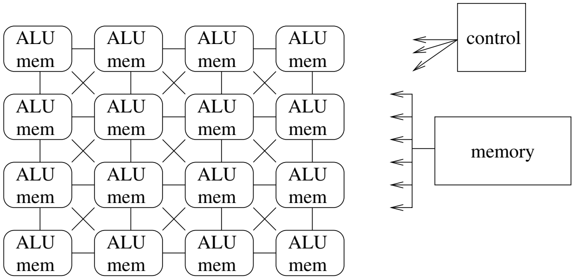

Array with diagonal connections

Classifications

Arrays

The CPUs are in SIMD lockstep as before, but now in an array

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More expensive than vector processors and much less common

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Arrays

Early array processors were very simple, but they became bigger as technology advanced

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		CPU	#CPUs	mem/CPU
DAP	1979	1 bit	4k	4k bits
CM	1983	1 bit	64k	few kB
MPP	1983	1 bit	16k	1 kB
MasPar	1990	4 bit	16k	16kB
MasParII	1992	32 bit	64k	64kB

DAP: ICL Distributed Array Processor
CM: Connection Machine (pretty lights)
MPP: Goodyear Massively Parallel Processor

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Vector/array processing processors are important due to their influence on the design of GPUs

Classifications

Arrays

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But others have been tried, with varying levels of success

Classifications

Pipelines, Systolic Arrays

Similar looking to vector processors, but actually quite different, are *systolic arrays*

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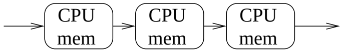

Process pipeline

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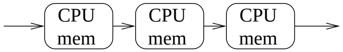

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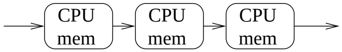

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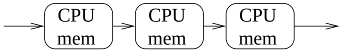

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Exercise Could this be classified MISD?

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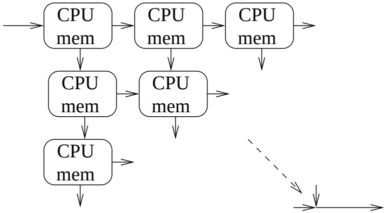
Part of the reason why digital TV is delayed relative to realtime is that the encoding of the picture goes through a big pipeline before it is transmitted: there is an inherent *latency* in pipelines

Classifications

Pipelines, Systolic Arrays

Systolic arrays are the obvious extension



Systolic array

but it is unclear if these were ever built

Classifications

Extensions of von Neumann

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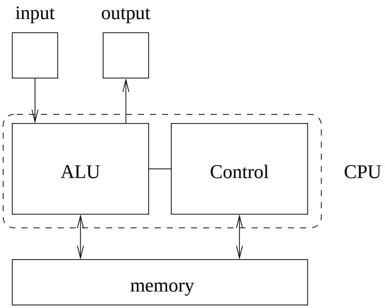
Is there a model that encapsulates multiprocessors in the same way?

There are many contenders, but no obvious winner

Classifications

Extensions of von Neumann

We have the original von Neumann 5 box model

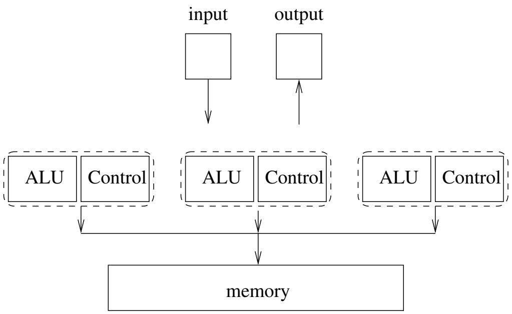


von Neumann 5 box model

Classifications

Extensions of von Neumann

Shared memory MIMD

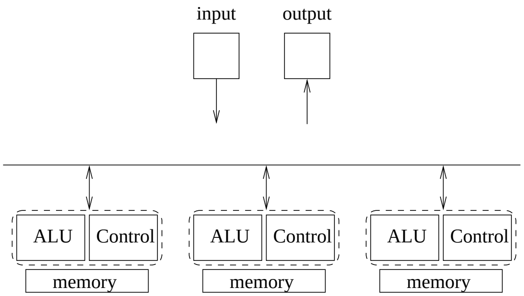


Shared memory box model

Classifications

Extensions of von Neumann

Distributed memory MIMD

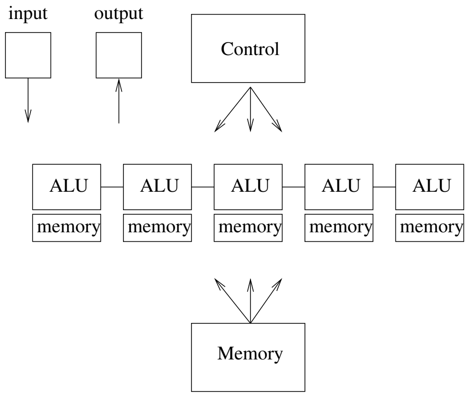


Distributed memory box model

Classifications

Extensions of von Neumann

Vector processor



Vector processor memory box model

Classifications

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Classifications

Extensions of von Neumann

Perhaps there just isn’t a single extension of von Neumann that is suitable as a one-size-fits-all solution

Or perhaps we just haven’t thought of it yet?

Classifications

Extensions of von Neumann

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Extensions of von Neumann

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As with von Neumann, the idea is that you

- write your program in accordance with the model
- the model maps well onto all kinds of real hardware
- therefore your program maps well onto all kinds of real hardware

Classifications

Extensions of von Neumann

Firstly: **PRAM**

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- *Exclusive Read Exclusive Write* (EREW). Each memory location can only be read or written by *one* processor at a time. The simplest architecture
- *Concurrent Read Exclusive Write* (CREW). Each memory location can be read by many processors simultaneously, but written by just *one* processor at a time (c.f. global memory in a vector processor)

Classifications

Extensions of von Neumann

- *Concurrent Read Concurrent Write* (CRCW). Each memory location can be read or written by *many* processors simultaneously. Not a realistic model

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- *Exclusive Read Concurrent Write* (ERCW). The fourth combination, never used.

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Extensions of von Neumann

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- Memory is unlimited. This assumption is also often made in analysis of uniprocessor algorithms

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And people want to run programs on datasets of ever-increasing size

Classifications

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But it gives you a rough idea and it is extensively used in analysis of parallel algorithms: we'll have some examples later

Classifications

Extensions of von Neumann

Next: **BSP**

Classifications

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The *Bulk Synchronous Parallel* model

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Classifications

Extensions of von Neumann

Next: **BSP**

The *Bulk Synchronous Parallel* model

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It assumes processors with local memory communicating over a network

Good for distributed, but can be used for shared memory where you just have smaller communication costs

Classifications

Extensions of von Neumann

A computation is modelled as a sequence of *supersteps*

Classifications

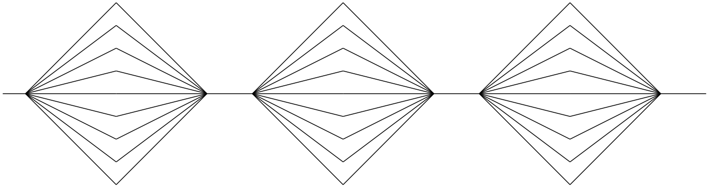
Extensions of von Neumann

A computation is modelled as a sequence of *supersteps*

- each processor does some computation (MIMD, but could be SIMD)
- each processor does some communication
- each processor waits at a global *barrier* until everybody has finished their communications. This is the “bulk synchronous” part
- repeat

Classifications

Extensions of von Neumann



BSP supersteps

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More realistic than PRAMs, but harder work to get analyses out of it

But those analyses tend to be a better match to realistic hardware

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Extensions of von Neumann

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This might be the source of the confusion in parallel hardware, but we have to live with it

Analysis

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They are quite crude, but effective

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Or a parallel *implementation* with a corresponding sequential implementation: by timing actual running code

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We have seen that having p processors won't necessarily make our program run p times as fast

Analysis
Speedup

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Or a parallel *implementation* with a corresponding sequential implementation: by timing actual running code

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Ideally we'd like $S_p = p$, but this never happens

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But speedups can improve for a larger computation where the *relative* cost of communications drops

Remember clusters are used for large problems where the emphasis is on size, not speed

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This is more common than we'd like