Topics

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Each year this unit is given may cover different topics so don’t be too worried if past exam papers ask questions on things that were not covered this year

Hardware

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But there has been hardware support for parallelism for much longer than you might think

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But there has been hardware support for parallelism for much longer than you might think

Even in sequential CPUs!

Hardware

Bit level

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More complex and expensive hardware, but faster

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A simple example, but this illustrates how parallelism trades complexity for speed

Hardware

Pipelines

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Again from Architecture: instructions are executed faster by using a pipeline

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This is parallelism by overlapping the fetch$\rightarrow$decode$\rightarrow$fetch arguments$\rightarrow$execute$\rightarrow$store result cycle

Hardware

fetch→decode→args→exec→store→fetch→decode→args
→exec→store→fetch→decode→args→exec→store→fetch
→decode→args→exec→store…

Hardware

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becomes

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It also shows how simple CPU clock speed is *not* a good indicator of speed of processing

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                                              …
```

Again, more complexity for speed

It also shows how simple CPU clock speed is *not* a good indicator of speed of processing

A pipelined CPU will produce results faster than a non-pipelined CPU of the same clock speed

Hardware

Coprocessors

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This allowed a weak form of parallelism: ship an operation (say a square root) off to the coprocessor, and while it is chewing on that, the main processor can carry on with something else in parallel

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Exercise Read about *Tensor Processing Units* (TPUs)

Hardware

Superscalar

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Simultaneous execution of whole instructions is called *superscalar*

Pipelining is parallel execution of *parts* of the instruction cycle

Hardware

For example, the two adds in

```
x1 = y1 + z1;
x2 = y2 + z2;
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can be done at the same time

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The CPU needs to sort out the dependencies to determine if it can do simultaneous multiple operations

Hardware

Out of Order

This can be improved with careful *instruction scheduling* by the processor, to let it do *out of order execution*

For example, the code

```
x1 = y1 + z1;
a1 = x1*y1;
x2 = y2 + z2;
```

is equivalent in results to

```
x1 = y1 + z1;
x2 = y2 + z2;
a1 = x1*y1;
```

but on a CPU with two add units the latter can do the two adds in parallel

Hardware

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But, mostly, this is a hardware feature

Hardware

Out of Order

But we have already seen how out of order execution can break parallel code if we are not careful

Hardware

Out of Order

Hard Exercise (come back to this later). Suppose we have initial values `x = 0` and `y = 1`. Two parallel threads on hardware that does out of order execution:

Thread 1	Thread 2
`y = 3;`	`if (x == 1) {`
`x = 1;`	`    y = 2*y;`
	`}`

What are the possible final values of `y`?

Example taken from the Rust website; also see
`https://en.wikipedia.org/wiki/Memory_ordering`

Hardware

Hyperthreading

Hardware

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In that case one thread will have to pause and wait

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The amount of repetition in the architecture will imply some limits on how effective this is and how much parallelism can be gained, as will the pattern of memory accesses by the code

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Most High Performance systems turn off hyperthreading (a bigger share of the memory cache is more important than more threads)

Hardware

SWAR

Next: the idea of SIMD/vector processing has been adopted in a small way in the instruction sets of some processors

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Now we can regard a 64 bit register as

- a 64 bit register
- two 32 bit registers
- four 16 bit registers
- eight 8 bit registers

Hardware

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An instruction is provided to (for example) add together eight 8 bit values in those registers in parallel

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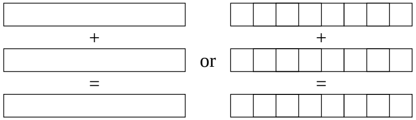

SIMD Within A Word

Hardware
SWAR

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We are treating the register as a (small) vector processor

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Similarly others from other manufacturers (AMD, Arm, etc.)

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In fact, few languages support SWAR operations directly, so there has to be some mechanism for getting to SWAR from conventional code

The process of converting sequential operations to SWAR is called *vectorisation*

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SWAR

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For a compiler spotting that a loop can be converted into SWAR vector instructions is very hard

Hardware
SWAR

For example, the multiplies in the code

```
char x[20], y[20];
for (i = 0; i < 20; i++) {
  y[i] = x[i]*x[i];
}
```

might be compiled as *three* ($8 + 8 + 4$) 8-way SWAR multiply instructions

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Plus a bunch of other stuff to get the values in and out of the right places in the register

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SWAR

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A lot of code to use these kinds of instructions still has to be written by hand, in assembler

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SWAR

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In contrast, in the functional style we write code like “do this operation on these data” (map), which is much easier to analyse as the operation is explicitly separate from the iteration

Hardware

SWAR

Exercise Think about the code

```
char x[], y[];
for (i = 0; i < n; i++) {
  y[i] = x[i]*x[i];
}
```

where the loop limit is variable

Exercise Then think about the functional version

```
y = x.map(square);
```

Hardware

VLIW

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This is strongly reliant on the compiler being good enough to understand and exploit the details of the RISC architecture

But this is easier than a compiler trying to make best use of a complicated CISC architecture

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VLIW

The same idea was touted for the *very long instruction word* (VLIW)

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Design a processor with many repeated arithmetic units—lots of add units, lots of multiply units and so on

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Have instructions that are *very long*, e.g., 128 bits or more

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Design a processor with many repeated arithmetic units—lots of add units, lots of multiply units and so on

Have instructions that are *very long*, e.g., 128 bits or more

The instructions are composites of the simple operations, e.g., two adds, a subtract and a multiply could be bundled together in a single instruction

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The compiler composes these instructions and makes sure there are no nasty interactions between the sub-instructions, e.g., none of the inputs to the sub-instructions are the outputs of any others of the sub-instructions

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The compiler does the hard work of sorting out interactions, leaving the hardware to blast on at full speed without checking or doing any reordering

The compiler is promising to the hardware that nothing bad is going to happen if the hardware blindly executes the instructions as given

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Compilers were not sufficiently clever to untangle enough instruction dependencies to get good hardware utilisation

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VLIW

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They called it *Explicitly Parallel Instruction Computing* (EPIC), a limited form of VLIW

It, too has flopped

Possibly due to their classic x86 chips being too entrenched, but also their compiler was never quite up to the job

Hardware

VLIW

It still pops up here and there: some AMD Radeon graphics chips have a VLIW architecture, though their newer architectures reverted to more traditional RISC

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VLIW may well re-emerge in the future when compilers have progressed further: though more likely it will be overtaken by other kinds of hardware parallelism

Hardware

VLIW

Exercise Think about the

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char x[], y[];
for (i = 0; i < n; i++) {
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example with VLIW

Hardware

Multicore

Next we have full replication of arithmetic units, control and registers: true multicore

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But, as we have seen, it’s not

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Modern multicore processors, having cores on the same chip, can share things like on-chip cache memory and other chip infrastructure

Also there is faster inter-core data transfer: no need to go off-chip. Off-chip transfers run at the bus speed, much slower than the chip speed

Hardware

Multicore

Large machines tend to be multiple multicores: e.g., two 24-core chips on a motherboard; a total of 48 threads of execution

Hardware

Multicore

Large machines tend to be multiple multicores: e.g., two 24-core chips on a motherboard; a total of 48 threads of execution

Or 96 if 2-way hyperthreading is enabled

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This is slightly *asymmetric*: some cores are a little “closer” to each other than the others

Hardware

All of the above

These things are not mutually exclusive

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A typical large installation these days is a CLUMP

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- a cluster

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A typical large installation these days is a CLUMP

- a cluster
- of multiple processors

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- a cluster
- of multiple processors
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- a cluster
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- and SWAR instructions
- on a pipelined architecture

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- each having multiple cores
- which might have hyperthreads
- and SWAR instructions
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- sometimes with a coprocessor or two on the side

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- which might have hyperthreads
- and SWAR instructions
- on a pipelined architecture
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It is very hard to make efficient use of all that!