GPUs

CUDA

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Similarly, there is a limit on the number of threads per block: up to 65536 in one of the above GPUs

GPUs

CUDA

GPUs offers a huge amount of processing power at low cost, but in a way that is extremely sensitive to memory access

GPUs
CUDA

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It is easy to get started with CUDA as it is basically C, but you do have to be very aware of the properties of memory

GPUs
CUDA

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Exercise Is this a good idea?

GPUs
CUDA

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Exercise Is this a good idea?

(Shortly we will see some systems that have physically shared memory)

GPUs
Memory

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And, if possible, overlap data transfers with GPU and CPU computation

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But a recent trend is to integrate the GPU onto the same package as the CPU (or vice-versa!)

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But a recent trend is to integrate the GPU onto the same package as the CPU (or vice-versa!)

Using lots of transistors!

GPUs

Memory

For example, AMD’s Kaveri is a CPU+GPU on the one chip

GPUs

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4 CPU cores and 512 GPU cores that share cache and main memory

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This is an example of a *Heterogeneous System Architecture* (HSA)

GPUs

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GPUs
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In a similar way, Apple's M1 architecture has CPU and GPU *and memory* on the same chip, further confusing the memory vs. compute costs question

GPUs

CUDA

Back to CUDA

GPUs
CUDA

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Here is an example of trivial CUDA code, `prog.cu`

GPUs
CUDA

Back to CUDA

Here is an example of trivial CUDA code, `prog.cu`

(Checking return values and tidying up omitted for brevity)

CUDA

```
#include <stdio.h>
__global__ void setarray(int p[])
{
  int k = blockIdx.x * blockDim.x + threadIdx.x;
  p[k] = k*k;
}
int main(void)
{
  int i, *dm, m[1024];
  cudaMalloc(&dm, 1024*sizeof(int));
  setarray<<<16,64>>>(dm);
  cudaMemcpy(m, dm, 1024*sizeof(int),
             cudaMemcpyDeviceToHost);
  for (i = 0; i < 1024; i++)
    printf("m[%d] = %d\n", i, m[i]);
  return 0;
}
```

GPUs

CUDA

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Each invocation of `setarray` gets the same pointer to some global memory allocated on the GPU

Each computes a different value for the index `k`, and each sets a different element of the array

This assignment is a memory bottleneck that will take a relatively long time to complete

GPUs

CUDA

CUDA programmers try to mitigate the memory bottleneck by ensuring there are lots of threads

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These run (in SIMD) until they would have to wait for a lengthy memory access to complete: the assignment to `p` in the example

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CUDA

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Within a block, a warp of 32 threads is scheduled to run

These run (in SIMD) until they would have to wait for a lengthy memory access to complete: the assignment to `p` in the example

Rather than simply waiting for the memory, this warp is put aside *while the memory access is still progressing* and another warp (from this block or another block on the same multiprocessor) is scheduled to run instead

GPUs
CUDA

Thus keeping the multiprocessor busy computing

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When the memory access has completed, the original warp can be run again

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Exercise Compare with hyperthreading as a way of keeping CPUs busy

GPUs
CUDA

Thus we want a lot of threads to schedule between as they run then wait for memory

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Ideally each block should have a multiple of 32 threads, whenever possible, to get the most from the multiprocessor

For example, running just 16 threads means half of the warp is lying idle

GPUs

CUDA

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GPUs
CUDA

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So we want at least as many blocks as multiprocessors, to keep all the hardware busy

Thus it's good to have lots of threads per block and lots of blocks per multiprocessor to provide lots of choice of warps to schedule

GPUs

CUDA

How many blocks and how many threads per block?

GPUs

CUDA

How many blocks and how many threads per block?

It depends on how the program accesses memory: e.g., the use of shared resources like block shared memory might be a factor

GPUs
CUDA

From the NVIDIA documentation:

- How many blocks?
  - At least one block per SM to keep every SM occupied
  - At least two blocks per SM so something can run if block is waiting for a synchronization to complete
  - Many blocks for scalability to larger and future GPUs
- How many threads?
  - At least 192 threads per SM to hide read after write latency of 11 cycles (not necessarily in same block)
  - Use many threads to hide global memory latency
  - Too many threads exhausts registers and shared memory
  - Thread count a multiple of warp size
  - Typically, between 64 and 256 threads per block

GPUs
CUDA

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And to add to the complexity: later versions of CUDA allow multiple different kernels to run concurrently (i.e., it schedules between kernels), so supplying more blocks and more threads to keep the hardware busy

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CUDA kernels run asynchronously from the CPU

GPUs

Memory Coalescence

And the *pattern* of global memory access is vital, too

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The memory bus has a high latency, but a large bandwidth

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We have to wait a long time for bytes to arrive; but then they arrive in large chunks

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Memory is set up to deliver, say, 64 bytes at a time (512 bit bus)

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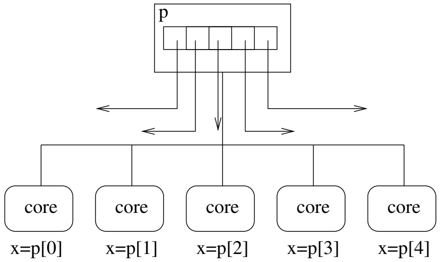
So a warp could be satisfied by just two reads

GPUs

Memory Coalescence



```
x = p[me]
```

If the reads are nicely arranged, a single read supplies many cores simultaneously: this is memory access *coalescence* (as discussed earlier in vector architectures)

GPUs

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If you get it wrong, it can be 16 times as slow

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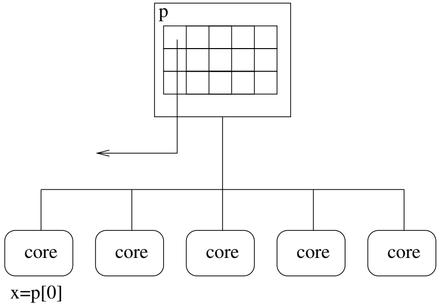

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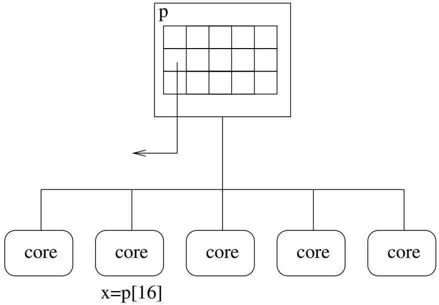

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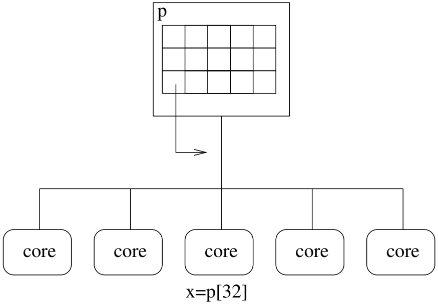

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GPUs

Memory Coalescence

In this case, it might be faster to read coalesced chunks of memory into the block shared memory, and then have cores read their values from there

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Awkward coding, but this is how you can get good performance

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__global__ void setarray(int p[])
{
  int k = blockIdx.x * blockDim.x + threadIdx.x;
  p[k] = k*k;
}
int main(void)
{
  int i, *dm, m[1024];
  cudaMalloc(&dm, 1024*sizeof(int));
  setarray<<<16,64>>>(dm);
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  for (i = 0; i < 1024; i++)
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GPUs
CUDA

Back to the example: `dm` is the address of a chunk of memory on the device

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The device memory is separate from the CPU memory, so we need special functions to allocate memory on the device

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The device memory is separate from the CPU memory, so we need special functions to allocate memory on the device

And we need explicit copies to get the data in and out of the coprocessor

GPUs
Memory

As always, data copies are time consuming, so we want to minimise them relative to computation time

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The reverse is also true: if the data are on the GPU, it can be faster overall to use one of the wimpy GPU cores for a computation rather than copy back and forth to the CPU

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This kind of computation vs. data movement judgement happens a lot when programming GPUs

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Real code would either simply have more blocks, or would interrogate the device to see how many multiprocessors it has and adjust accordingly

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Exercise but you wouldn’t want more than 32 blocks in our small example. Why?

GPUs

GPUs are becoming an ever more important method of computation

GPUs

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Even in phones: ARM’s Mali GPU now has OpenCL support

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GPUs are good for phones as they give a good amount of processing power for only a small amount of energy used

GPUs
OpenCL

OpenCL takes a wider view of computation than CUDA

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OpenCL is provided as a library that is callable from standard C (and other languages), thus not needing a special compiler

GPUs
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Much like the shader code in OpenGL and the like

GPUs

OpenCL

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Current OpenCL compilers produce code that runs universally but at sometimes uninspiring speeds (so code still needs the machine-specific tuning that OpenCL was supposed to avoid)

And there are features in the OpenCL programming model that reveal that the designers were still thinking of GPUs underneath the supposed genericity