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Formation of a porous alumina electrode as a low-cost CMOS neuronal interface

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ABSTRACT

A low-cost electrode design has been devised for drug discovery pharmacology, neural interface systems, cell-based biosensors and electrophysiology research, based on high volume CMOS (complementary metal oxide semiconductor) integrated circuit technology. The electrode is formed by the anodisation of CMOS metallisation to form nanoporous alumina. The process was developed to address the concern of aluminium neurotoxicity, improve corrosion resistance under physiological conditions and to present a preferential morphology for cell–substrate adhesion.

Thin-film anodisation is optimised to overcome problems of thermal fusing, enabling a variety of substrate morphologies to be produced using potentials of 10–100 V. Current density scaling factors are shown to confirm the suitability of CMOS circuit geometries to the anodisation process. Corrosion tests demonstrate improved corrosion performance of the porous alumina electrode. The process and scaling factors are validated by anodisation of a simple CMOS device.

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1. Introduction

Drug discovery pharmacology, neural interface systems, cell-based biosensors and electrophysiology research are key applications of neuron stimulation and recording. Currently, commercial devices exist primarily for research platforms and are custom-built by the deposition and patterning of conducting and insulating films on glass substrates. These designs require investment in expensive micro-fabrication facilities and result in high product cost. A prerequisite to establishing neuron stimulation and recording in the above markets will be to significantly reduce the product manufacturing costs. An alternative to custom fabrication is to exploit high volume CMOS (complementary metal oxide semiconductor) integrated circuit technology which forms the basis of most commodity electronic products. Through this route, the manufacturing costs of electrode products are potentially considerably lower, thereby enabling market growth.

Whilst CMOS is a potentially attractive solution, the neurotoxicity of aluminium persists as a topic of much debate [1,2]. One method to address this concern has been devised [3] where the aluminium is covered using additional deposition and patterning at the backend of the CMOS fabrication process. However, these post-processing steps reintroduce a reliance on micro-fabrication facilities which increase production costs.

Electroless plating of gold onto the CMOS aluminium has also been investigated [4]. This approach is of notable merit due to its simplicity and ability to meet a low-cost criterion. However, the process may require further development to eliminate defects in the deposited coating that risk causing rapid galvanic corrosion of the aluminium [5,6].

1.1. Electrode material

Aluminium forms the conventional basis for high volume integrated circuit (IC) metallisation and this is likely to continue for the foreseeable future. Mature CMOS processes that are likely to be used for small quantity production of biocompatible electrodes, such as for multiple electrode arrays (MEAs), are typically >0.1 μm gate length processes. The transition to copper metallisation may not be totally complete for niche applications until 45 nm gate length processes are reached [7–9].

1.2. Electrode morphology

It has been found that nanoporous morphologies formed in silicon wafers can create a basis for CMOS electrodes [10,11]. Sapelkin et al. [12] etched CMOS ICs to form porous silicon (pSi) structures which were found to be biocompatible and to which cells exhibited preferential adhesion. Unfortunately, access to the silicon substrate on standard CMOS technology is only possible by etching directly through the metallisation and interlayer insulation layers. This also exposes the active regions (those areas of an IC substrate

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where transistors are formed) to the physiological medium (i.e. *in vivo* extracellular medium or *in vitro* cell culture medium), which results in rapid degradation of the circuits due to ionic contamination [13]. Moxon et al. [14] used pSi in fabricated MEA electrodes without adhesion promoters and confirmed that the nanoporous electrode surface displayed better biocompatibility than a smooth surface, illustrated by the increased growth of neurites and the reduced adhesion of astrocytes (glial cells). Similar results were also reported in Ref. [15] where axons extended preferentially on pSi with pores between 150 and 500 nm rather than smooth silicon, small pores (100 nm) or large pores (1500 nm). With the exception of Low et al., the above studies evaluated porous substrates without the use of adhesion molecule coatings. These would have otherwise modified the nature of the surfaces under investigation.

1.3. Aims of paper

As a result of the published research on pSi it is possible that there may be preferential adhesion to nanoporous alumina formed by anodising CMOS aluminium metallisation. This could have the advantages of providing a porous morphology similar to that of the pSi, combined with the benefit of converting the electrochemically active aluminium metal into bioinert alumina. Previous work has been reported on neuron cells cultured on porous alumina, but the substrates were either coated with cell adhesion molecules (which affect electrical performance [16]) or were not configured as electrodes [17,18]. Others have evaluated non-neuronal cell types on porous alumina, in particular osteoblasts, and showed good biocompatibility [19–23].

This paper introduces a novel low-cost technique to modify standard CMOS circuits to create electrodes based on nanoporous alumina. The feasibility of constructing such electrodes using CMOS is explored. The aim is to determine whether such an approach can form a foundation for various electrode designs. We examine the simplest design scenario of a cell positioned above open pores that are filled with physiological medium, but we anticipate this foundation may also lead to other designs such as created by electrodeposition into the pores. Validation through stimulation and

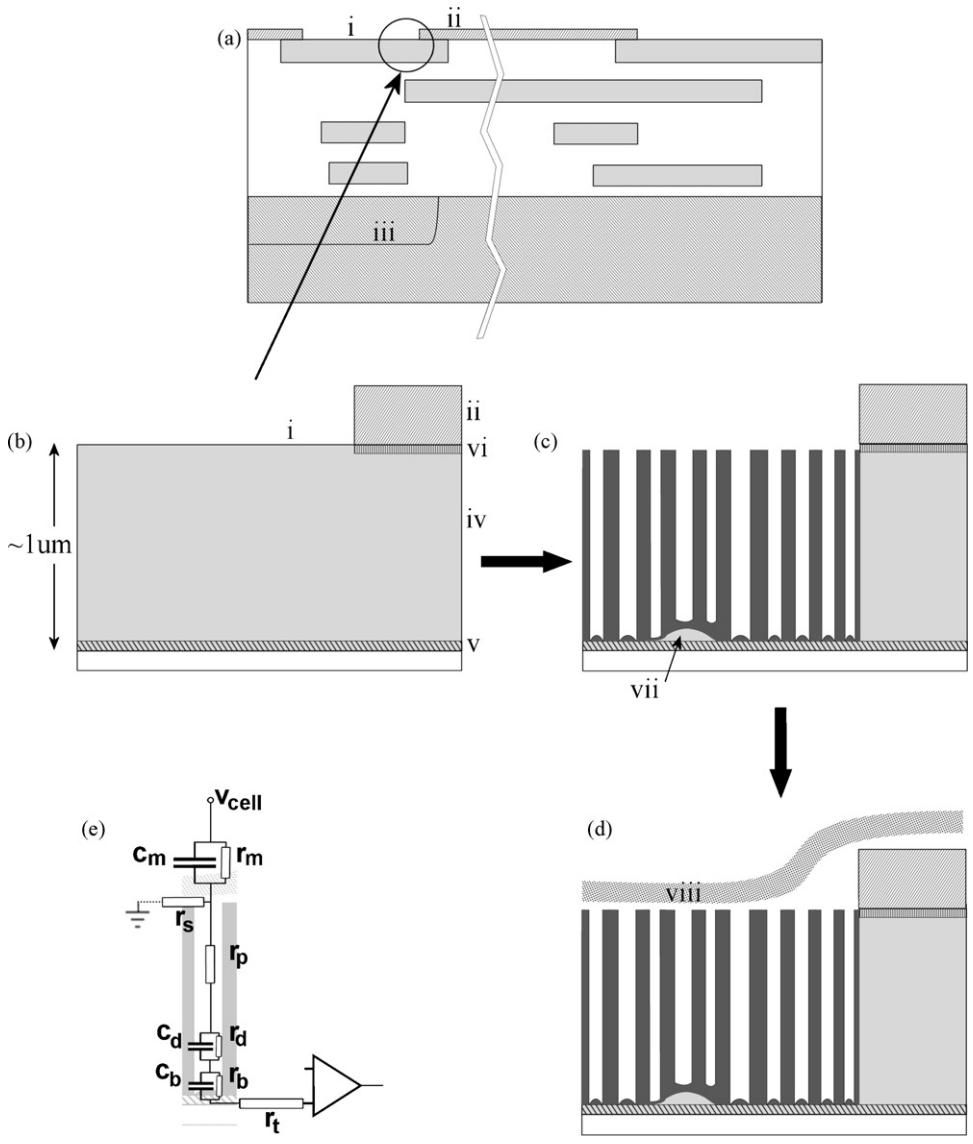

Fig. 1. Formation of electrode. (a) Section through a typical CMOS IC process showing 'pad' openings to form electrodes (i), on the uppermost of the metal layers (four shown here), with passivation layer (ii), and transistor area (iii), within the silicon substrate. (b) Enlarged view of electrode area showing the metallisation, comprising of aluminium alloy (iv), with titanium barrier layer (v), and anti-reflective coating (vi). (c) Modified electrode formed by anodisation, with remnants of aluminium (vii) remaining unanodised. (d) The adherent neuron cell membrane (viii), forms a seal with the top of the pores. (e) Electrical model for a single pore element and input into high impedance amplifier.

recording with a working electrode array will be required but is not included at this stage since it will depend on the actual design built from the porous alumina foundation.

A simplified section of a CMOS device before modification is shown in Fig. 1a. The electrode areas are formed by openings (i) in the passivation layer (ii). Transistors are constructed at the silicon substrate surface (iii). Fig. 1b shows detail of the aluminium metallisation material (iv) to be anodised. This is typically 1 μm thick and usually includes a small proportion of copper (typically 0.5 wt.%) to inhibit electromigration [13,24]. During the elevated temperatures of IC fabrication, 'contacts' formed by depositing aluminium directly onto a silicon substrate tend to alloy at their interface. The underlying semiconductor (p–n) junctions near to this silicon–metal interface can be damaged by spikes of aluminium penetrating them. This phenomenon, 'contact spiking', is usually eliminated by depositing aluminium that has been alloyed with silicon (typically 1–2 wt.%) and by including a 'barrier layer' of titanium, titanium nitride or titanium–tungsten [24] below the aluminium (Fig. 1b(v)) to separate it from the silicon in contact areas. Additionally, it is frequently necessary to include an anti-reflective coating (ARC), often titanium nitride, on top of the aluminium to facilitate photolithography (vi).

1.4. Electrode concept

In order to demonstrate the plausibility of the proposed electrode design, it is necessary to consider its physical and electrical structure. Anodisation of the aluminium CMOS pads to form porous alumina can ultimately produce the structure shown in Fig. 1c. Unless the duration of anodisation is greatly extended, remnants of aluminium film often remain (vii). The neuron–alumina junction (Fig. 1d) forms a wet electrode below the cell membrane (viii): the electrode is formed via the low impedance alumina pores filled with physiological medium, through the impedance at the pore base (anodic barrier oxide) and to the high impedance transistor gate input. The design relies on sufficient conductance through the base of the alumina pore to enable the recorded action potential to be sensed at the CMOS transistor gate and vice versa for stimulation.

Fig. 1e shows a simplified electrical model for one element (one pore): the intracellular potential, v_{cell}, is coupled to the electrode via the cell membrane impedance, c_m and r_m: the seal resistance element, r_s, represents the lateral leakage path from the extracellular space below the cell membrane to ground. (The extracellular medium is grounded through a bath electrode.) These electrical characteristics have been investigated elsewhere [25–28]. Maximising resistance r_s is critical to forming a good electrical junction between cell and electrode, as demonstrated in Ref. [29]. To achieve this without using mechanical manipulation of cells, the height of this 'cleft' must be minimised by good cell adhesion.

The resistance r_p represents the physiological medium in the pore. Due to the relatively high conductivity of the medium (typically 10^3 S m^{-1} [17,27]), r_p is small, even for long pores formed by anodising the entire 1 μm of aluminium.

A double-layer impedance is formed at the solid–solution interface [30] for which a simple equivalent circuit is usually sufficient and comprises of a capacitance c_d and resistance r_d [31]. With action potential characteristic frequencies, f, in the order of 1 kHz it has been shown that the magnitude of the impedance $(2\pi f c_d)^{-1}$ that results from the double-layer capacitance typically dominates resistance r_d by a factor of 10^3 to 10^5 [32,33].

For a nanoporous alumina film in a physiological medium or other electrolyte, it is the anodic barrier layer impedance at the base of the alumina pore space that governs the overall electrical characteristics of the film [34,35]. During the formation of the nanoporous layer the anodic barrier oxide layer at the base of each pore is of high impedance, defined by c_b and r_b [35–37]. However, where a thin film has been completely anodised, the characteristic hemispherical pore base is deformed [38] and the barrier oxide impedance reduces, becoming resistive, and defined solely by r_b. The impedance of the pore base can also be decreased by electrodeposition of a noble metal [39], by thinning of the barrier oxide by a post-anodisation etch, or by electrochemical thinning [40–42].

A further consideration is that the pore walls of insulating alumina do not contribute to the active area of the electrode. Defining the proportion of pore area to wall area as porosity, P, then for very thin walls P approaches unity and the active area approaches the total electrode area. As P decreases the electrode impedance is expected to increase and with $P = 0$ the pores would be non-existent so that the electrode becomes an insulator. It is also expected that the lateral seal resistance of the cleft will scale with porosity: since the cleft height is much less than the pore height the lateral impedance across the pore can be considered negligible compared to the lateral resistance along the cleft between the top of the pore walls and cell membrane. The seal resistance is then expected to be proportional to $1 - P$. With $P = 0$ the seal would represent the whole of the adhered membrane surface area as in the case of a conventional planar electrode. A poor seal resistance may therefore be anticipated for highly porous films where P approaches 1. The above suggests there will be a trade-off between good seal resistance and good coupling through the base of the pores and that extremes of porosity are likely to produce particularly poor electrical performance.

Below the porous alumina barrier oxide, the titanium barrier layer, together with any residual aluminium ((vii) in Fig. 1c), forms a conductor to the periphery of the electrode, r_t. Sufficient conductance of this layer for stimulation and recording is assured since anodisation can only occur by conduction through the layer, i.e. the decrease in conductance that occurs towards the end of thin-film anodisation becomes self-limiting. The electrode is then connected to the IC circuit, i.e. the elecotroneurogram (ENG) amplifier or driver, through the standard low impedance CMOS metal tracks.

The above description demonstrates that is possible to measure changes in intracellular potential, v_{cell}, using this electrode configuration. The methods to form the nonporous alumina electrode will now be described.

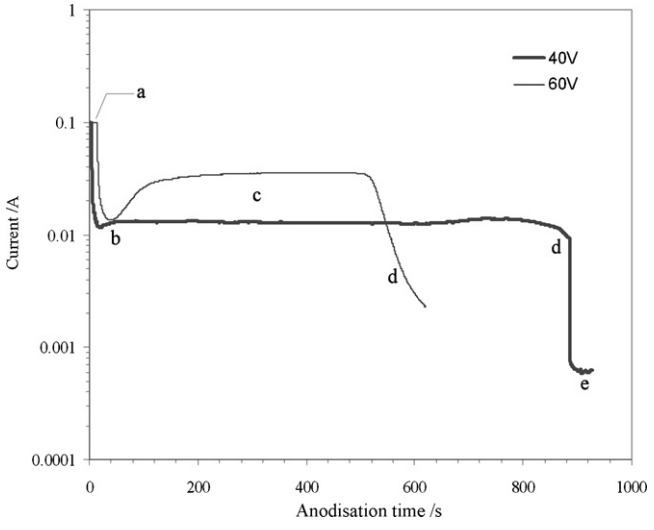

Fig. 2. Typical anodisation of 960 nm aluminium thin films (2 wt.% oxalic acid, 40 and 60 V, 10 °C, on 40 nm Ti and glass substrate. Anodised area, $A \approx 400$ mm^2): barrier forming (a); barrier completion (b); porous layer growth (c); aluminium film consumed (d); leakage current (e).

2. Experimental methods

In order to avoid the difficulties of evaluating working electrodes of small geometries (typically 7×10^{-4} mm^2), the relevant CMOS metal layers were initially reproduced on glass substrates, providing surface areas of 10 mm^2. Glass coverslips were coated (Teer Coatings, UK) to represent a typical CMOS metallisation (austriamicrosystems AG, 0.8 μm process). The upper metal layer was reproduced by depositing ~40 nm of titanium followed by ~960 nm of aluminium (99.5% purity). The coverslips did not have an upper titanium nitride ARC since during CMOS fabrication this layer is removed from the pad areas when etching the passivation.

2.1. Thin-film anodisation

A simple apparatus was used, comprising an open glass beaker containing 4 wt.% phosphoric acid electrolyte, magnetic stirrer, platinum gauze cathode and the coated coverslip suspended using a miniature crocodile clip. The anodisation bias was provided by a Keithley 236 Source-Measure Unit operated by a PC running a custom Labview 7.1 (National Instruments) program. The software enabled easy selection of either potentiostatic or galvanostatic anodisation, bias ramping, and datalogging of the respective current or voltage. The anodisation potential defines the anodic 'cell' size—the spacing between adjacent pore centres (and to avoid confusion with references to biological cells, we always refer to this spacing as either 'anodic cell size' or 'pore pitch'). With thick (bulk) substrates of optimised electropolished aluminium the established relationship – the 'anodisation ratio' – in a 4% phosphoric acid electrolyte is 2.5–2.7 nm V^{-1} [43] but such a ratio has not been established for anodisation of thin films. Nevertheless, by adjusting the anodising voltage it is possible to produce a variety of anodic cell sizes. Potentiostatic anodisation was generally used to give a pore pitch constant throughout the layer since galvanostatic anodisation would give a branching pore structure not conducive to a simple electrode design [43]. It is also possible to vary the anodic cell size by selecting different electrolytes but our selection of phosphoric acid enabled the largest anodic cell sizes for a given anodising voltage [44].

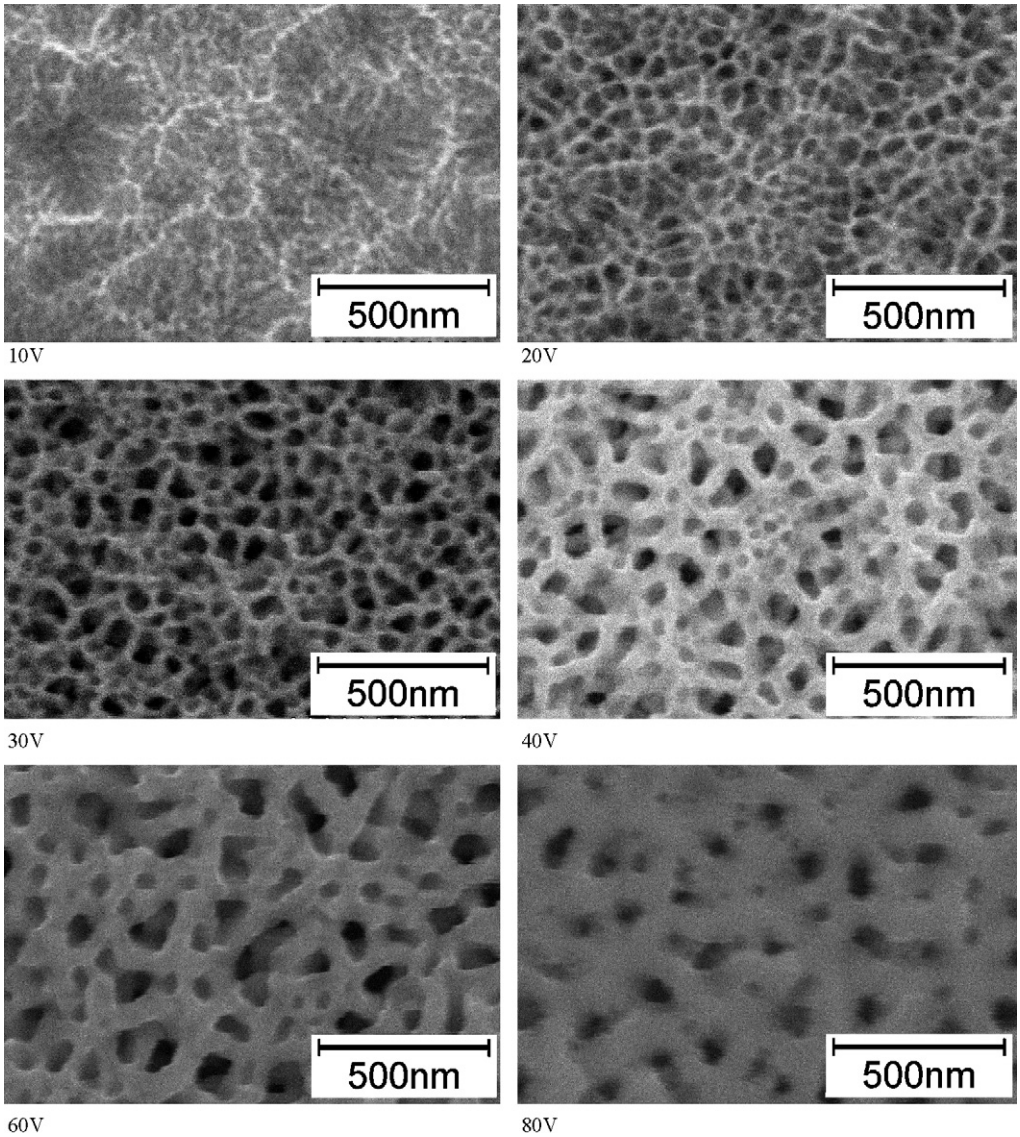

Fig. 3. Scanning electron microscope (Hitachi S-4300) images of porous alumina films produced at the stated anodisation voltages (40, 60 and 80 V substrates are shown prior to pore widening).

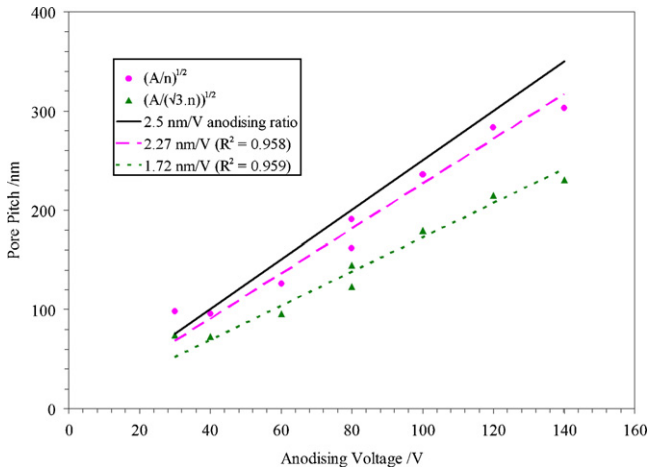

Fig. 4. Fit of measured pore density data to the two models of anodic cell size (with area of image, *A*, and number of pores, *n*). The generally accepted 'anodisation ratio' of 2.5 nm V^{-1} is shown for reference.

Fig. 2 shows characteristic current–time curves for anodising under potentiostatic conditions at 40 and 60 V. During period (a) the barrier layer is formed and the current is limited by the maximum current of the supply (0.1 A). During period (b) the barrier layer growth is completed and the porous layer begins to form, leading to an increase in the anodisation current. Period (c) is steady-state porous layer growth. As the pores reach the base of the aluminium film, the current falls (d). The 40 V anodisation curve shows that continuing to apply bias after the aluminium is consumed results in a steady-state leakage current (e).

During initial setup of the apparatus it was observed that a complication of anodising thin aluminium films is thermal fusing of the metal due to high current densities. This was solved by three modifications. Firstly, the electrolyte temperature was lowered to 10 °C by immersing the beaker containing electrolyte within a larger outer beaker containing coolant (3% (v/v) ethylene glycol). A coil hand-formed from 6 mm diameter copper tube was submerged in the coolant and a primary circuit of coolant was pumped through the coil using a constant temperature bath and circulator (RTE-101, ThermoNeslab Instruments Inc.). Secondly, the phosphoric acid electrolyte was diluted with 25% (v/v) ethanol to prevent localised burning at the pore bases and to improve the coolant properties of the electrolyte [45]. Thirdly, the entire aluminium coated coverslip was submerged in the electrolyte by soldering a sheathed wire to the centre of the coverslip (Carrs 'Grey Label' flux and Carrs 'No. 179' solder) and insulating the connection ('TRV', Electrolube, UK).

2.2. Pore widening

To produce alumina films with morphologies similar to the biocompatible porous silicon and alumina substrates of the work outlined previously, the pores of the 40, 60, 80 and 100 V anodised substrates were widened. A standard method for pore widening was used which involved a simple post-anodisation etch using the 4% phosphoric acid solution [17,18,46–49]. At 45 °C the mean rate of dissolution was found to be approximately 9 nm min^{-1} allowing fast modification of the pore size.

2.3. Corrosion tests

CMOS ICs were fabricated using a standard double poly double metal 0.8 μm gate length process (austriamicrosystems AG). The ICs contained an array of 48 circular aluminium pads of 30 μm diameter and were assembled in 48 pin dual-in-line packages with removable lids. Glass cylinders were bonded to the package tops to form culture chambers and the bondpads and bondwires insulated using a silicone elastomer (Silastic 9161 RTV, Dow Corning). The culture chambers were filled with Krebs buffer solution (NaCl 118 mM, $NaHCO_3$ 25 mM, KCl 4.8 mM, KH_2PO_4 1.2 mM, $MgSO_4$ 1.2 mM, glucose 11 mM, $CaCl_2(2H_2O)$ 1.5 mM) and the ICs incubated at 40 °C in an air environment. Aluminium coverslips were also tested under these conditions.

3. Results and discussion

3.1. Aluminium coated coverslips and anodic cell size analysis

Porous substrates of various morphologies were successfully produced on the coverslips coated with titanium and aluminium (Fig. 3). The anodic cell size for each morphology was analysed to test whether it conformed to the 2.5 nm V^{-1} anodising ratio that is generally accepted for thick aluminium substrates. For the study of highly ordered porous layers this task is simplified by the regularity of the pores. However, the disordered nature of simple anodised layers (as in Fig. 3) makes this task more complex. It was therefore necessary to use image analysis software (ImageJ [50]) to calculate the mean anodic cell size from the scanning electron microscope (SEM) images. With an irregular pore structure there is no single method for determining which pores are adjacent. Two models were considered:

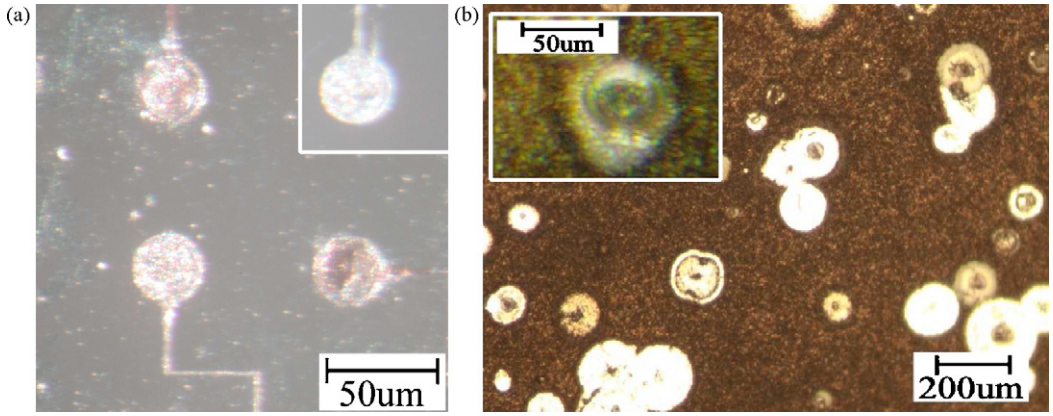

Fig. 5. Corrosion of aluminium after exposure to physiological medium, 40 °C, 48 h: (a) CMOS IC electrode pads are discoloured (diameter = 30 μm). For reference the inset shows a non-corroded electrode that was not exposed to medium; (b) discoloured coverslip surface with localised brightening at corrosion pits. The inset highlights a pit with a ring characteristic of hydroxide precipitate.

(i) assuming a regular square layout of pore centres, the mean anodic cell size, d, is $(A/n)^{1/2}$, where A is the area represented by the image being processed and n is the number of pores within that image.
(ii) if a hexagonal pore structure is assumed, as expected for highly ordered films, $d = (A/(\sqrt{3} \cdot n))^{1/2}$.

The above models (with n ranging from 48 to 461) yield the anodic cell sizes shown in Fig. 4 revealing anodisation ratios of 1.72–2.27 nm V^{-1}. Possible reasons for the smaller than expected anodisation ratios are as follows: firstly, there are limitations in the models in that pores do not conform to the assumed regular spacing and so there is difficulty in establishing the inter-pore boundaries. This is the case for both automated image processing and manual analysis. Pores may also branch and merge considerably along their length through the alumina film. A more regular pore structure has been achieved by others through refinements such as preparing the surface with electropolishing [51], using a two-step anodisation process [52] and by starting with higher purity metal than the 99.5% used by us to date [43]. We may expect to see such irregularities in the typical Al–1.0% Si–0.5% Cu CMOS metallisation. Future work will study this alloy in order to understand the effects of the alloying materials. Secondly, the smaller anodisation ratio could be a result of the potential drop across the substrate length due to the higher resistivity of the thin film compared to a thick aluminium substrate. Thirdly, it could be due to limitations of the basic two-electrode configuration, resulting in loss of applied voltage at the cathode and in the electrolyte.

3.2. Corrosion of aluminium and anodised substrates

The non-anodised CMOS ICs and the aluminium coated coverslips that had been stored in Krebs buffer were inspected after 48 h. Many of the IC pads and all aluminium coated coverslips had a discoloured brown appearance. Fig. 5a highlights the localised discolouration of the IC pads. Fig. 5b shows that the discolouration of the aluminium coated coverslips was much more generalised. Further examination showed pitting corrosion on both the IC pads and the aluminium coated coverslips. The inset of Fig. 5b shows prominent precipitate deposition forming a ring around a pit and is characteristic of hydroxide precipitate associated with this corrosion mechanism. Pits are known to initiate at localised defects on the surface, such as flaws in the native oxide, and are frequently activated by aggressive ions such as the chlorides present in the Krebs solution [53]. No corrosion was seen on any of the porous alumina coated coverslips that had been tested in Krebs buffer. This demonstrates the effectiveness of the anodisation as protection against corrosion.

3.3. Scaling factors

Having established that the coverslip metallisation can be successfully anodised, it is now necessary to confirm that the maximum voltage and current ratings of a CMOS circuit are not exceeded. Firstly, the appropriate configuration of the IC during anodisation allows the large anodisation potential to be dropped solely across the oxide at the aluminium–electrolyte interface and therefore this does not present an electrical overstress hazard to the underlying active CMOS components. Secondly, the current density is independent of the surface area to be anodised, i.e. the anodisation current is proportional to the anode (IC pad) area. The relationship between two different areas is simply $I_1/I_2 = A_1/A_2$, where I_x are the anodising currents and A_x are the respective anodising surface areas. With a coverslip anodising area of $A_1 = 400$ mm^2, a circular CMOS electrode area of radius, r, of 15 μm ($A_2 = \pi r^2$) and a peak coverslip anodising

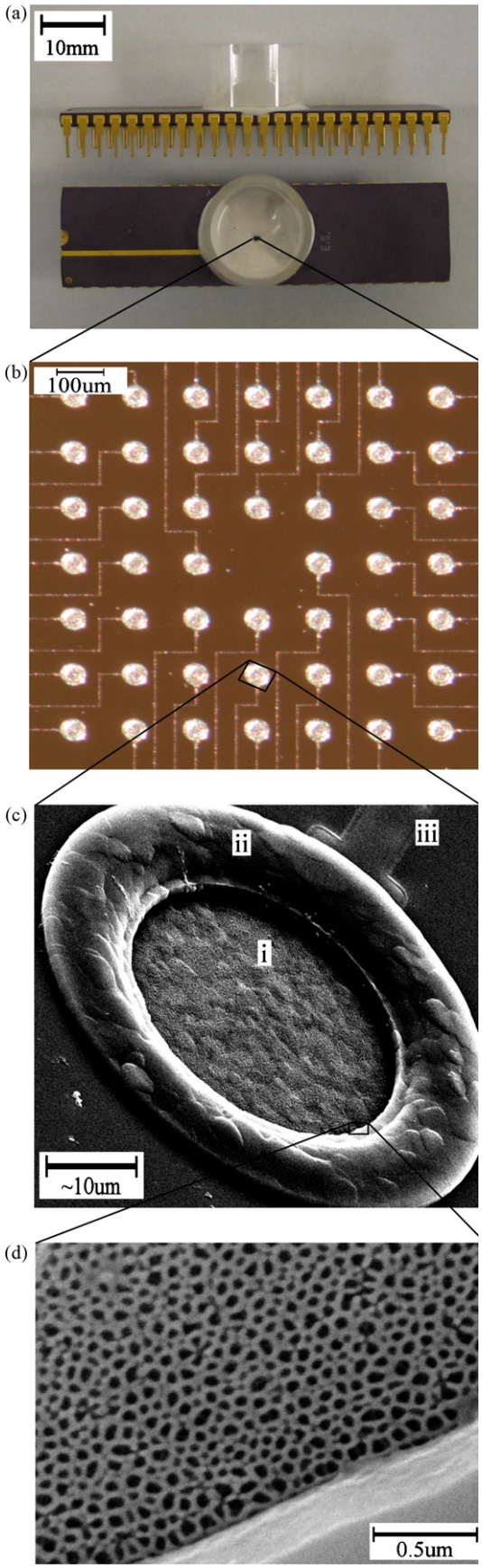

Fig. 6. Anodising of CMOS pad: (a) assembled IC with culture chamber and exposed pad array; (b) array of 48 pads; (c) SEM image of a single pad, tilted 55° ((i) electrode surface; (ii) passivation rising over outer edge of metal; (iii) metal track connection); (d) an anodised pad (30 V, 4% phosphoric acid, 22 °C), with passivation at lower right.

current of 100 mA for $V \leq 100$ V, the peak CMOS current for one pad is estimated to be 177 nA.

For the simple IC design discussed above where tracks connect to one side of each pad, the maximum track width is the same as the electrode diameter, i.e. 30 μm. By applying typical design rules and process parameter limits such as maximum current density (0.8 μm gate length process [54]), the maximum current capacity of the 30 μm track is 84 mA. This represents an excellent margin to the 177 nA peak anodisation current. For simultaneous anodisation of an array of electrodes, the current can be sourced through the usual supply rail, assuming maximum ratings for the supply are not exceeded.

3.4. IC anodisation

The CMOS IC with an array of 30 μm diameter pads was anodised at 40 V using a 4% phosphoric acid electrolyte in the culture chamber. This preliminary IC design was not optimised for anodisation and had metal tracks between bondpads and electrodes of only ~2 μm wide. To avoid fusing these tracks, the large initial current flow during barrier oxide formation was limited by ramping the potential to 40 V over 30 s. SEM analysis confirmed correct anodisation of the IC (Fig. 6). This demonstrated that standard CMOS metal tracks are capable of carrying sufficient current to electrode pads undergoing anodisation and substantiates the current scaling model discussed above.

Further work is being conducted to characterise and optimise electrode conductivity and to enhance the CMOS IC design for anodisation. Biocompatibility and cell adhesion tests are also forthcoming. It will be necessary to investigate the porosity trade-off between seal resistance and electrical coupling through the base of the pores and compare performance to planar metal electrodes. A final electrode design will then enable validation by means of stimulation and recording of mammalian neuronal cells.

4. Conclusion

A low-cost processing method has been devised to overcome the biocompatibility and corrosion limitations of unmodified CMOS electrodes. Glass coverslips with CMOS-like metallisation have been successfully anodised and the thin-film anodisation process characterised. Scaling factors have shown that the currents are sufficiently small to allow 30 μm CMOS IC pads to be anodised, and this has been confirmed by successfully anodising a passive CMOS electrode array. It has therefore been demonstrated that the approach developed provides a controlled and low-cost method of fabricating CMOS multiple electrode arrays with good corrosion resistance and a nanoporous morphology conducive to good cell adhesion.

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