Sensors and Actuators B 147 (2010) 697–706

Contents lists available at ScienceDirect

Sensors and Actuators B: Chemical

journal homepage: www.elsevier.com/locate/snb

Nanostructured electrodes for biocompatible CMOS integrated circuits

Anthony H.D. Graham[a,*], Chris R. Bowen[b], Jon Robbins[c], Georgi Lalev[d], Frank Marken[e], John Taylor[a]

[a] Department of Electronic & Electrical Engineering, University of Bath, Bath, BA2 7AY, UK
[b] Department of Mechanical Engineering, University of Bath, Bath, BA2 7AY, UK
[c] Receptors & Signalling, Wolfson CARD, King's College London, London SE1 1UL, UK
[d] Manufacturing Engineering Centre, Cardiff University, Cardiff CF24 3AA, UK
[e] Department of Chemistry, University of Bath, Bath, BA2 7AY, UK

ARTICLE INFO

Article history:
Received 26 January 2010
Received in revised form 10 March 2010
Accepted 11 March 2010
Available online 17 March 2010

Keywords:
Electrode
CMOS
Anodic aluminum oxide (AAO)
Biocompatibility
Impedance
Biosensor

ABSTRACT

This paper reports on the adaptation of standard complementary metal oxide semiconductor (CMOS) integrated circuit (IC) technology for biocompatibility, enabling a low-cost solution for drug discovery pharmacology, neural interface systems, cell-based biosensors and electrophysiology. The basis for the process is the anodisation of IC aluminium electrodes to form nanoporous alumina. The porous alumina was electrochemically thinned to reduce the alumina electrode impedance. For applications where a porous electrode surface is either preferred or acceptable, we demonstrated that porosity can be manipulated at room temperature by modifying the anodising electrolyte to include up to 40% polyethylene glycol and reducing the phosphoric acid concentration from 4% (w/v) to 1%. For applications requiring a planar microelectrode surface, a noble metal was electrodeposited into the pores of the alumina film. Limited success was achieved with a pH 7 platinum and pH 5 gold cyanide bath but good results were demonstrated with a pH 0.5 gold chloride bath which produced planar biocompatible electrodes. A further reduction in impedance was produced by deposition of platinum-black, which may be a necessary additional step for demanding applications such as neuronal recording. During this work a capability for real-time electrochemical impedance spectroscopy (EIS) was developed to study anodisation, barrier oxide thinning, oxide breakdown and electrodeposition processes. To study the pore morphology, focused ion beam (FIB) was employed to produce cross-sectional cuts of the IC features which were inspected by SEM with an 'In-lens' detector.

The anodisation process and the optional electrodeposition steps require only simple bench equipment operated at room temperature and is therefore a viable route for manufacturing low-cost biocompatible electrodes from standard CMOS ICs.

1. Introduction

The concept of using standard complementary metal oxide semiconductor (CMOS) integrated circuit (IC) technology for biological sensors is appealing due its ubiquity and low cost. Potential markets for such sensors include drug discovery pharmacology, neural interface systems, cell-based biosensors and electrophysiology research tools [1]. Unfortunately biological environments are often damaging to IC components—the semiconductor industry spent decades developing passivation and packaging technologies to keep electronic components separate from hostile external environments. In principle, electrodes can be formed by opening the IC passivation to form windows onto the aluminium conductors below, this being standard practice where bondpads are formed to allow off-chip connection via bondwires. However, a pivotal issue has been the difficulty in exposing the standard aluminium metal to biological media. Our previous work has confirmed that aluminium electrodes corrode in cell culture media [2]. For research purposes additional microfabrication can be undertaken in a cleanroom environment to deposit biocompatible platinum electrodes on top of the passivation but this may make products prohibitively expensive if scaled to high volume sensor production. In ref. [2] we demonstrated the feasibility of low-cost post-processing that can convert the electrochemically active aluminium to biocompatible nanoporous alumina by anodisation. It was demonstrated that the electrical potential and currents required for this process were compatible with CMOS technologies. We proposed that several potential electrode designs were feasible: the porous alumina could be used directly as the electrode or the pores could be filled with a noble metal to form an electrochemically stable and biocompatible planar surface. This paper shows how the electrical characteristics of a porous alumina electrode can be optimised by thinning the alumina barrier oxide that underlies the porous layer. We study

* Corresponding author. Tel.: +44 0 1225 386071.
E-mail addresses: abmahdg@bath.ac.uk, abmahdg@agraham.me.uk (A.H.D. Graham).

0925-4005/$ – see front matter © 2010 Elsevier B.V. All rights reserved.
doi:10.1016/j.snb.2010.03.030

the anodisation of the CMOS aluminium alloy and show how this is different from anodisation of pure aluminium substrates.

As presented in ref. [3], it may be desirable to modify the surface porosity for cell-based porous alumina electrodes to improve adhesion. For this previous work, a phosphoric acid anodising electrolyte was selected to enable flexible one-step anodisation at voltages between 20 V and 120 V resulting in inter-pore distances up to ~300 nm. This was achieved at room temperature, without burning and avoiding high current densities that are incompatible with the CMOS implementation. Electropolishing [4] and two-step anodisation processes [5] are not practical with the CMOS metallisation due to the layer's limited thickness of ~1 μm. The phosphoric acid electrolyte had been demonstrated to be biocompatible, enabling good cell vitality and cell-substrate adhesion. The work had therefore established that the surface chemistry resulting from the anodisation in phosphoric acid was suited to this application: surfaces produced using other anodisation electrolytes such as oxalic and sulphuric acids remain less well characterised with respect to cell culture. Lower porosities can also be achieved by using oxalic or sulphuric electrolytes, but anodising at voltages up to 120 V requires the temperature to be lower than room temperature to avoid burning and high current density [6]. This would require cooling apparatus that does not fit well with our objective of developing a low-cost manufacturing process. We have therefore extended the work of Chen et al. [7] on pore size manipulation using polyethylene glycol (PEG) by changing their 15 °C experiment condition to 21 °C. This same technique also enables lower anodising voltages to be used (i.e. voltages that are more readily implemented in CMOS) for a given porosity. Additionally, we present a novel method of measuring the electrode impedance in real time during anodisation and electrodeposition.

2. Experimental methods

The overall process investigated was to convert aluminium electrodes which corrode in cell culture media to bio-inert porous alumina by anodisation, then reduce the impedance by thinning the alumina barrier oxide. For some applications such as neuronal recording, a low impedance electrode is required to minimise Johnson noise. Therefore, to further reduce impedance or to provide a planar electrode surface, filling the pores with a noble metal was studied. To reduce cost and avoid difficulties with analysis of microelectrodes (typically 700 μm^2), preliminary experiments were performed on coated glass coverslips with metal layers that matched the metallisation of CMOS ICs. Later experiments were performed using CMOS ICs with an array of 48 planar microelectrodes.

2.1. Coverslip fabrication

The relevant CMOS metal layers were reproduced on 22 mm × 32 mm glass substrates, coated (Teer Coatings, UK) to represent the same CMOS metallisation as the ICs (austriamicrosystems AG, 0.8 μm process). This comprised ~40 nm of titanium followed by ~960 nm of aluminium alloy (Al–1.0 wt%Si–0.5 wt%Cu). The glass coverslip substrate performed a similar role to the interlayer dielectric (i.e. the insulator that separates metal tracks) of the ICs. For the evaluation of the influence of Si and Cu alloying elements on the vertical orientation of the nanopores, coverslips to be used as controls were similarly coated but with pure aluminium (99.9 wt%) instead of the alloy.

2.2. IC fabrication

Multiple electrode array (MEA) ICs were fabricated by austriamicrosystems AG, Germany, supplied in 48-lead ceramic dual-in-line packages (DIP) with removable die-cavity lids. These evaluation ICs were passive devices with no transistors: an array of 48 electrode pads, each 30 μm diameter and pitched 190 μm apart, was connected directly to the pins of the ceramic package (Fig. 1). Glass chambers were bonded to the top of the ceramic package and the bondwires isolated from the medium in the chamber by encapsulation using Silastic® 9161 (Dow Corning, UK) elastomer.

2.3. Anodisation

Unless otherwise stated, anodisation was performed at 30 V or 60 V using a 0.4 M (4%, w/v) phosphoric acid electrolyte at 21 °C. Anodisation at 60 V in 0.3 M oxalic acid electrolyte at 15 °C was used in the evaluation of pore structure (anodisation times are discussed in Section 2.6). Anodisation was performed by holding the coverslip in a miniature crocodile clip and submerging approximately 2 cm^2 of its length into the electrolyte. Porosity manipulation experiments were performed using coverslips in 0.05–0.4 M (0.5–4%) phosphoric electrolyte with 375 mM–2.0 M (15–80%, w/v) of PEG-400 (Sigma–Aldrich, UK) at 21 °C. Porosity was measured via image analysis using the open-source ImageJ software [8]. Platinum counter electrodes were used for all experiments: a 4 cm^2 mesh electrode for coverslips or 1 cm^2 plate electrode for ICs.

2.4. Stand-alone impedance spectroscopy

Measurements were taken at open circuit potential (OCP) and room temperature between 0.01 Hz and 10^4 Hz which has been shown to be sufficient to characterise porous alumina [9,10]. The electrochemical impedance spectroscopy (EIS) was performed

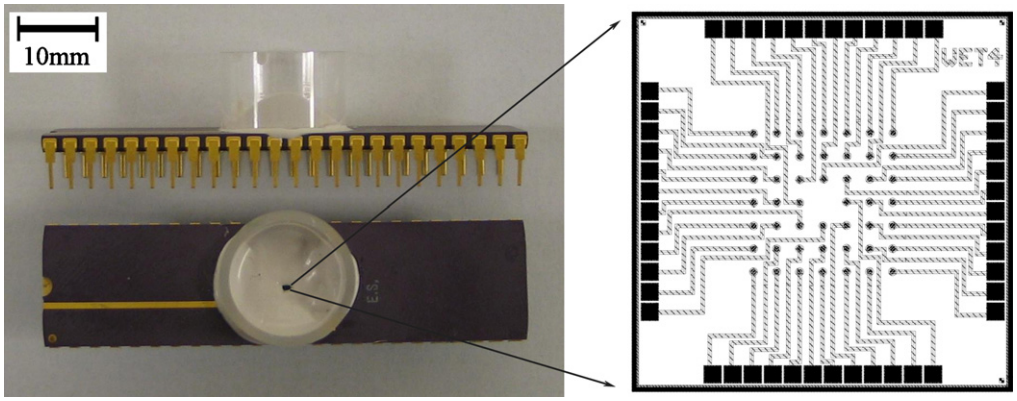

Fig. 1. An assembled CMOS device and schematic of the electrode array. Each of the 48 electrodes is connected directly to a pin of the ceramic package. The square IC has 3.2 mm sides.

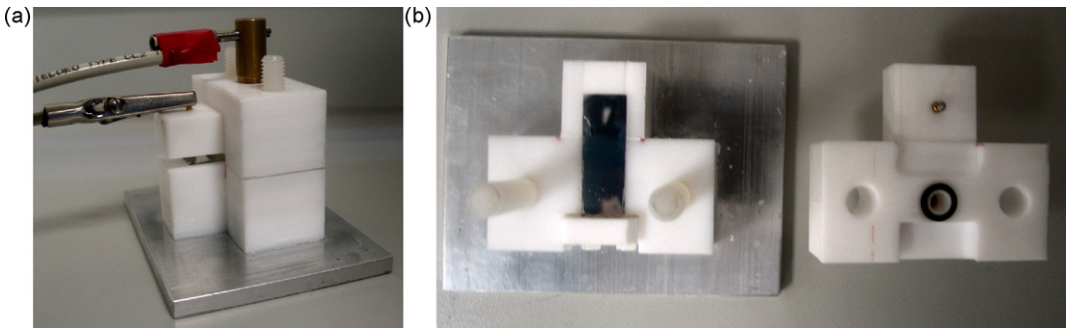

Fig. 2. EIS cell for coverslips: (a) coverslip under test; and (b) disassembled cell base (with coverslip in place) and cell top showing the O-ring that creates a substrate–electrolyte interface of 0.5 cm^2. The upper brass counter electrode has a clearance fit which allows it to be inserted until it contacts the electrolyte surface. The electrical connection to the coverslip is via a stainless steel needle point spring probe.

using a Solartron 1260A Impedance/Gain-phase Analyzer with 1296 Dielectric Interface, in a 0.6 M K_2SO_4 electrolyte. For coverslips, an EIS cell was devised as shown in Fig. 2 in which the substrate–solution interface has a known area. For EIS of ICs, connections were via the package pin(s) and a 1 cm^2 platinum plate counter electrode placed in the chamber.

2.5. Real-time impedance spectroscopy

It is common practice to record current and/or voltage versus time during anodisation [11,12] and also during electrodeposition [13]. Impedance measurements are usually restricted to 'before and after' characterisations. However, we are interested in how the impedance varies during anodisation of the thin aluminium film and during barrier oxide thinning (see below) and so devised instrumentation to record complex impedance as a function of both frequency and time. This was achieved using the iBasic scripting language of the Agilent 4294A Precision Impedance Analyzer. A block diagram of the apparatus is illustrated in Fig. 3. An external Keithley 2400 SourceMeter was controlled via the 4294A through the GPIB (IEEE-488) interface to enable high voltage (140 V) anodisations. A relay switch box allowed temporary isolation of the SourceMeter for the few seconds required to make an impedance sweep at OCP. Example programs are provided as supplementary data.

2.6. Barrier oxide thinning

Coated coverslips were first anodised at 60 V. The insulating barrier oxide between the pores and the titanium layer was then thinned either using an unbiased 'pore-widening etch' or by electrochemical thinning, the latter simply being anodisation whilst reducing the voltage either by stepping down the current or ramping the voltage. Several thinning schemes were investigated since this aspect is considered a key factor for successful electrodeposition [12]. The schemes were defined as:

1. 'Anodisation to cusp': 60 V was maintained until the anodisation current began to fall. It was postulated in [2] that this is the point where a small proportion of the pores have reached the titanium layer; as more pores reach the titanium layer the current falls further. Barrier oxide thinning was commenced when the current fell below 85% of the steady-state anodising current: this allowed a reasonable margin against false-triggering due to fluctuations in the steady-state anodising current.
2. 'Anodisation to completion': 60 V was maintained until the anodisation current fell to <10% of its steady state.
3. 'Partial anodisation': only approximately 50–70% of the aluminium film was anodised prior to commencing barrier oxide thinning. This provided highly conductive aluminium metal below the porous alumina so that comparisons could be made with other work using thick aluminium films [12,14], i.e. the effect of the thin 40 nm titanium resistance was eliminated for these experiments.
4. 'Pore-widening etch': after anodising using one of the above schemes, the substrate remained in the 4% phosphoric acid electrolyte, unbiased, whilst collecting impedance data. This method of barrier oxide thinning [15,16] was used in our experiments as

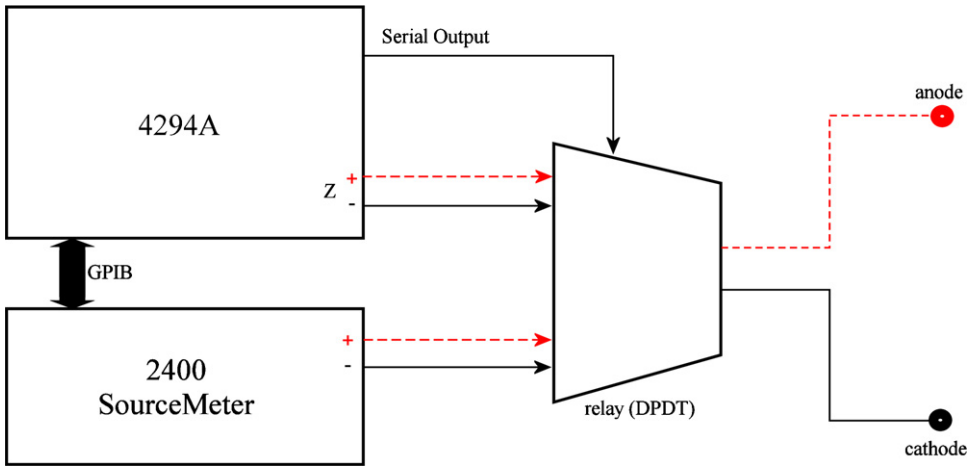

Fig. 3. Block diagram showing method for anodisation and real-time impedance measurement. The Agilent 4294A with the iBasic program acts as a master controller, driving the Keithley 2400 SourceMeter and double-pole-double-throw (DPDT) relay switch box. For anodisation, the anode output is connected to the coverslip or IC pins and the cathode is connected to the counter electrode in the electrolyte. For electrodeposition, the outputs are reversed with cathode connected to the coverslip or IC pins.

a control for comparison with the biased electrochemical thinning.

Voltage ramps were used rather than stepped or ramped current since the former were more readily scalable between the coverslip area and microelectrodes. Initial experiments on coverslips used linear voltage ramps. Exponential ramps were used for later coverslip experiments and IC anodisation as these better mimic the voltage decay during constant current thinning [12]. Duration of the ramps varied to ensure correct thinning of the barrier oxide (see Section 3.3): for anodisation in oxalic or 4% phosphoric acid at 21 °C, ramp duration between 30 V and 5 V was 300 s and for 60 V and 5 V was 600 s. Ramp times in 40% PEG between 30 V and 5 V were 1800 s, 780 s, 540 s and 360 s for 0.5%, 1%, 2% and 4% phosphoric acid, respectively.

2.7. Electrodeposition

Initial experiments used the pulsed electrodeposition (PED) scheme discussed in [17] which is tailored to baths with low metal ion concentrations, high aspect ratio porous films and minimises undesirable hydrogen gas evolution: this comprises a −70 mA cathodic pulse of 8ms, followed immediately by a +3 V anodic pulse of 2 ms, after which there is a zero bias recovery period. The waveform period is 100 ms. A circuit was constructed to generate this waveform (see supplementary data files for the circuit schematic) and so avoid the need for expensive industrial PED equipment. For later experiments, the Agilent 4294A was again used to measure impedance during electrodeposition and was also used to control a PED current generated directly by the Agilent 33220A waveform generator. For deposition onto IC microelectrodes, current density was controlled using 68 MΩ resistors in series with each pin, giving an approximation to individual and ideal current sources. With approximately 2.3 V as the measured potential across the system (cathode to anode) during PED, and with the resistors driven by a 10 V waveform from the 33220A, the expected current was $(10–2.3)/68 \times 10^6 = 113$ nA per electrode ($\equiv$16 mA cm^{-2} and comparable with the 20 mA cm^{-2} used for the coverslips).

Two principal platinum baths were used, as described in ref. [18]. Firstly, 16 mM (5.0 g l^{-1}) dinitrodiammine-platinum "P-Salt" $Pt(NH_3)_2(NO_2)_2$, (Strem Chemicals, UK) in a buffer of 674 mM disodium hydrogen phosphate dihydrate and 136 mM diammonium hydrogen phosphate, pH adjusted to 7.0 using NaOH or H_3PO_4 and operated at 35 °C. Secondly, 24 mM (1%) chloroplatinic acid (CPA) $H_2PtCl_6{\cdot}6H_2O$ (Sigma–Aldrich, UK) with 264 μM (0.01%) lead(II) acetate trihydrate operated at 21 °C or 45 °C. The CPA bath was also used for platinum-black deposition but operated at higher current density (100 mA cm^{-2}). Gold deposition was achieved using either 59 mM (20 g l^{-1}) gold chloride $HAuCl_4{\cdot}3H_2O$ (Sigma–Aldrich, UK) with 71 mM (7 g l^{-1}) H_2SO_4 (pH 0.5), or 26 mM (7.5 g l^{-1}) gold cyanide $KAu(CN)_2$ (pH ~5, Spa Plating, UK), both at 21 °C. A 1 cm^2 platinum counter electrode was used for all deposition experiments. A saturated calomel electrode (SCE) was used as a reference only during set up of the bath.

2.8. Microscopy

A Carl Zeiss 1540 XB system consisting of field emission scanning electron microscope (SEM) and focussed ion beam (FIB) was used for all analysis. The FIB enabled precision cross-sectioning of coverslips and processed IC pads using 2 nA current and energy of 30 kV. SEM images at 36° were taken after each FIB cross-section to inspect the sample morphology. The SEM "In-lens" detector provided not only high-resolution images but also gave a unique morphological contrast (e.g. electrodeposited metal grain structure), which further facilitated the analysis. Due to the close working proximity of the SEM column, ICs were first disassembled by removing the culture chamber and the white elastomer shown in Fig. 1.

3. Results and discussion

3.1. Effects of CMOS alloying elements on pore structure

Coverslips coated with titanium and pure aluminium were anodised in phosphoric acid at 30 V or 60 V. Coverslips coated with the titanium and Al–1%Si–0.5%Cu were processed identically, with additional coverslips anodised in oxalic acid at 60 V. ICs were also anodised at 30 V and 60 V. The cross-sections illustrated in Fig. 4 show the respective pore structures. Other studies of anodisation of aluminium containing higher proportions of alloying elements than CMOS show similar disruption to the pore growth [19–23]. Here we confirm this effect also applies to CMOS thin film metallisations with only 0.5% copper and 1.0% silicon. This effect is distinct from the more commonly observed disordered structure of pores at the surface – as viewed from the top – which is attributed to the lack of surface preparation (which is not practical with processing of CMOS ICs). The attributed cause of the pore disruption is substantiated by the fact that changing the anodising potential or using oxalic acid electrolyte did not alter the nature of pore growth. For neuronal recording sensors these interconnected pores may have a negative impact on the electrical performance as the model discussed in ref. [2] suggests the interconnects will result in reduced lateral impedance of the 'cleft' under the cell. Unfortunately, the CMOS metallisation comes from the foundry 'as is' and has been optimised for semiconductor reliability. Since the alloying elements cannot readily be reduced, applications such as neuronal recordings can use electrodeposition of a noble metal into

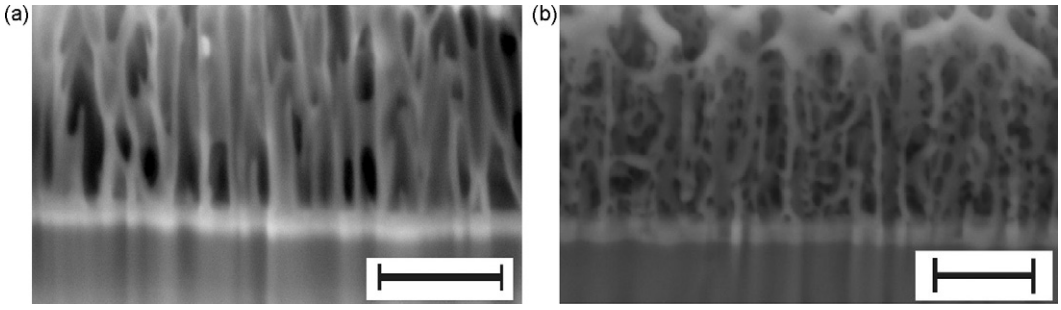

Fig. 4. SEM images taken at 36° after FIB cross-sectioning showing the effect of CMOS alloying elements on pore structure: (a) pure aluminium (99.9%) coverslip anodised at 30 V. The pore orientation varies slightly and so are not perpendicular to the FIB section surface. The length of uninterrupted pore wall therefore gives an indication of straightness; and (b) an Al–1%Si–0.5%Cu coverslip anodised at 30 V. The pore walls are interrupted by cross-linking to adjacent pores. The same pore structure was seen on alloy coverslips anodised at 60 V, for anodisation in oxalic acid and for CMOS microelectrodes anodised at 30 V and 60 V (c.f. Fig. 12(b) where the electrodeposition enhances the image definition of the pore structure). Scale bars are 500 nm.

the pores which may provide a more suitable surface, as discussed below.

3.2. Manipulation of surface porosity for cell adhesion optimisation

As discussed in Section 1, the addition of PEG to an electrolyte is expected to reduce the acid's pore-widening action during anodisation and so reduce the porosity of the film. This is a useful method for controlling surface porosity whilst maintaining room temperature processing and low voltage anodisation. Using 4% (w/v) phosphoric acid, there was no effect on porosity with addition of up to 60% (w/v) PEG-400. However, at 40% PEG, reducing the phosphoric acid concentration demonstrated the desired porosity manipulation: reducing the phosphoric acid concentration from 4% to 0.5% resulted in halving the surface porosity (Fig. 5). It was also observed there seems to be an upper limit to the usefulness of this technique since coverslips anodised with low (0.5%) phosphoric acid concentration or >50% PEG resulted in poor quality films exhibiting reduced porous alumina thickness. This was visible to the naked eye as pin-holes through the substrate and was confirmed by SEM. Cross-sections showed that the vertical orientation of the pore growth in the Al–Si–Cu alloy was not notably different to that of those samples anodised in 4% phosphoric acid. Therefore, by using 40% (w/v) PEG-400 with only 1% (w/v) phosphoric acid instead of the standard 4% (w/v) electrolyte, this room temperature method can be used to reduce surface porosity by up to ~47%. It is acknowledged that this work is very limited but is deemed sufficient to be implemented as a useful tool in the manufacture of the proposed biocompatible electrodes. Further work could be performed to fully characterise the effects of PEG concentration, electrolyte concentration and temperature.

3.3. Barrier oxide thinning

After anodisation the oxide film was subjected to thinning to decrease its electrical impedance. The anodising voltage and current versus time characteristics for the various barrier thinning schemes are illustrated in Fig. 6. This demonstrates the ability to control the system for 'cusp', 'completion', or 'partial' anodisation schemes, with linear or exponential ramps. It was noted that if the anodising voltage is reduced too quickly then the current drops sharply and the impedance reduction stalls. This is believed to be due to the barrier oxide having similar characteristics to a p–n junction [13,24]: anodisation requires the barrier oxide to be in a state of avalanche breakdown, as seen at high fields across a reverse-biased p–n diode. A bias magnitude below this threshold causes the current to cease. This is not a problem with current ramp barrier thinning schemes (since by definition the forced current maintains the required bias), but demonstrates that it is necessary to limit the ramp rate during voltage thinning schemes so that an anodisation current is maintained.

Fig. 7 shows $|Z|_{(f,t)}$ for an aluminium alloy coated coverslip anodised to 'cusp', with complex impedance, Z, versus frequency, f, and time, t. The initial data-point shows the impedance of the unmodified aluminium. The increasing impedance versus f is due to the double layer at the solid-solution interface [10]. The increased impedance during steady-state anodisation is due to the thick barrier oxide at the base of each pore, the thickness being approximately proportional to anodising voltage, 1.1 nm V^{-1} [25]. Prior to reaching the cusp in the current–time curve (Fig. 6a(i)), it is interesting to note that the impedance ($40\,\text{Hz} < f \leq 10^5\,\text{Hz}$) starts to rise further before any change in anodising (d.c.) current can be seen. The cause of this is not understood, but perhaps could be an indication of barrier oxide deformation when forming immediately above the titanium layer.

3.4. Pore-widening $|Z|$ versus t

To understand better the commonly-adopted pore-widening etch as a method for reducing barrier impedance, the impedance was recorded versus time during dissolution in 4% phosphoric acid at 21 °C. A pure aluminium coverslip was partially anodised at 30 V, without voltage ramp barrier thinning. The results are shown in

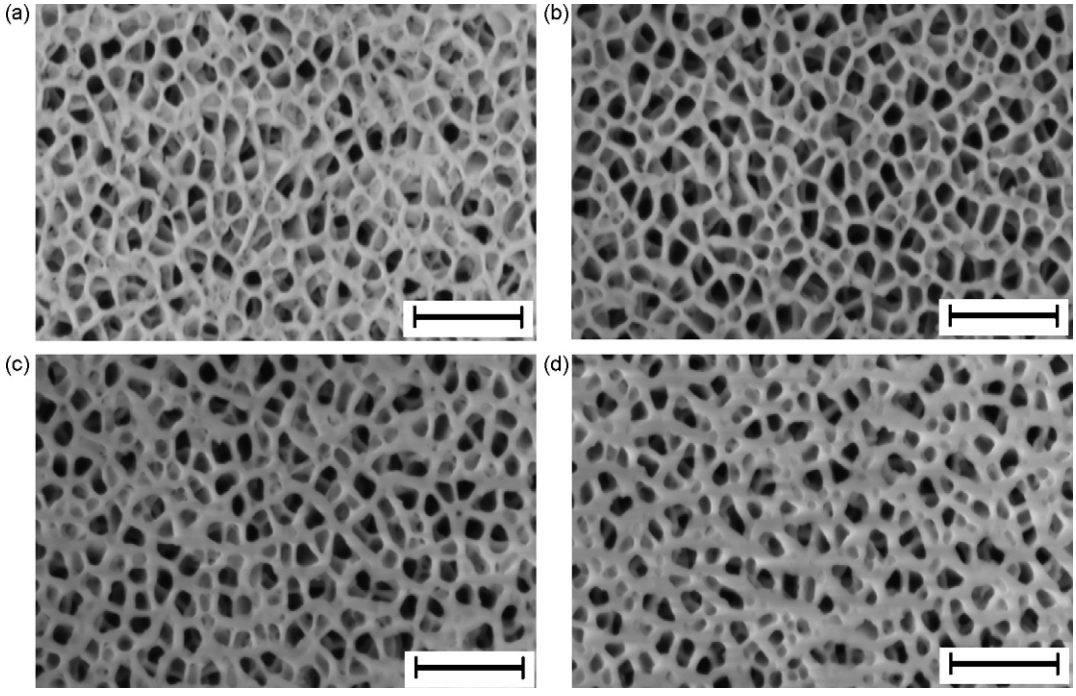

Fig. 5. SEM imaging (top view) showing the effect of surface porosity manipulation using 40% PEG-400 at 21 °C with varying acid concentrations (w/v): (a) 4% H_3PO_4; (b) 2% H_3PO_4; (c) 1% H_3PO_4; and (d) 0.5% H_3PO_4. Anodisation was at 30 V using coverslips. Porosities, measured using ImageJ software, are 68%, 48%, 36% and 32%, respectively. Scale bars are 500 nm.

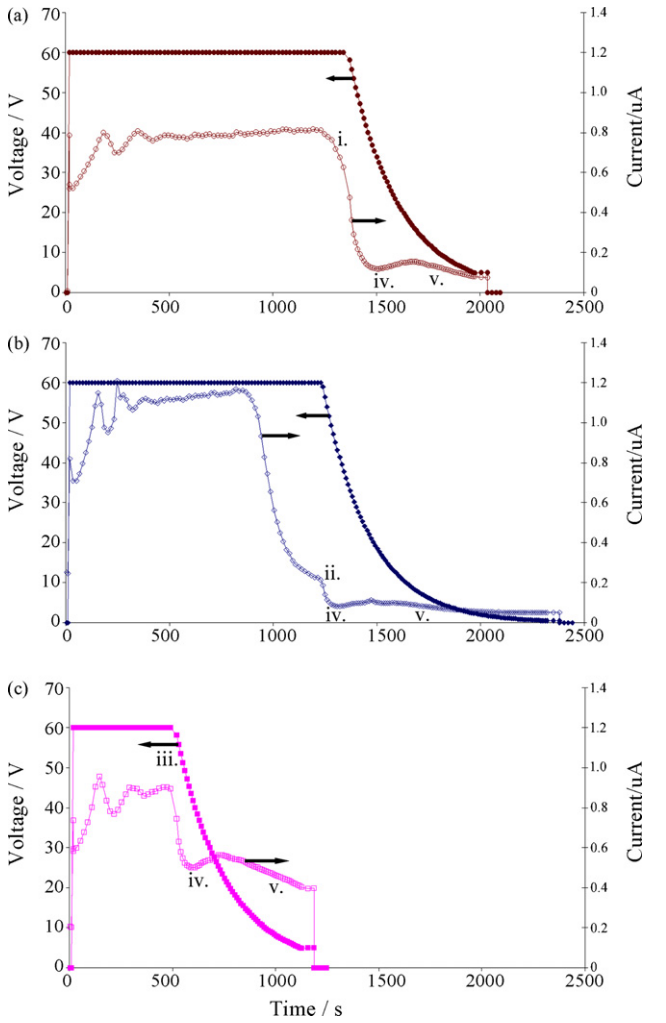

Fig. 6. Voltage and current versus time for the various anodisation and barrier thinning schemes: (a) 'cusp' – the exponential voltage ramp is triggered by a fall (i) of current from the steady-state; (b) 'completion' – the exponential voltage ramp is triggered (ii) when the anodisation current has fallen to 10% of its steady-state; and (c) 'partial' – the exponential voltage ramp is initiated after a fixed period (iii), calculated as 50–70% of the duration to the cusp. Drop off in currents during initial ramping (iv) indicate the barrier oxide temporarily falling out of the anodising breakdown state. The desired approximation to a linear current ramp can be seen in the latter stages of the voltage ramp (v). The arrows indicate the corresponding *y*-axis. Data are for a CMOS array of 48 electrodes with combined area of 3.4×10^{-8} m^2, anodised in 4% phosphoric acid at 21 °C.

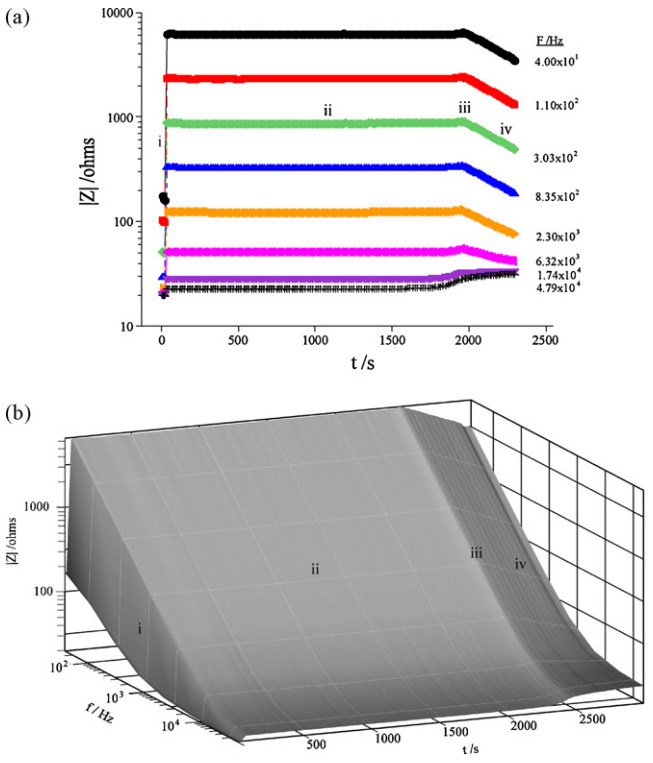

Fig. 7. Impedance magnitude, $|Z|$, versus frequency, f, and time, t, during anodisation to 'cusp' and voltage ramp thinning for a coverslip of area 2.0 cm^2. The same data are shown in 2D (a) and 3D (b): the impedance rapidly increases as the 30 V bias is first applied (i); the impedance remains constant during steady-state anodisation (ii); just prior to the 'cusp' the impedance starts to rise slightly at all measured frequencies (iii); during the voltage ramp the impedance decreases for $f \leq 10^4$ Hz (iv).

3.5. Electrodeposition

Deposition of a noble metal into the pores can be used to lower the electrode impedance or to provide a planar surface whilst maintaining electrochemical isolation of the aluminium. Plating coverslips and ICs with the neutral P-salt bath at 35 °C generated gas, was slow and resulted in poor deposits after terminating at 2 h. No improvement was noted either through increasing the duty cycle (i.e. the 'on time' proportion of the waveform) or increasing the platinum concentration of the bath by a factor of 10. It

Fig. 8 and, by correlation with optical appearance of the coverslip, it was confirmed that the linear decrease in impedance was due to barrier oxide thinning. This was followed by a rapid decrease in impedance due to the remains of the pore structure being etched. The remaining un-anodised aluminium then presents a planar surface of similar impedance to the coverslip prior to anodisation. After etching through the aluminium the impedance increases slightly as the 40 nm titanium layer is reached.

Prior to pore-widening the barrier oxide thickness resulting from the 30 V anodisation is approximately 33 nm (1.1 nm V^{-1}): Assuming the start of region e at 5722 s in Fig. 8 corresponds with complete removal of the barrier oxide, this indicates an oxide thinning rate of 33/((5722-328)/60) = 0.37 nm min^{-1}. Rates of 0.13 nm min^{-1} [26] for 5% (w/v) phosphoric acid and ~0.1 nm min^{-1} [27] are reported for room temperature dissolution. This method provides a useful tool for calculating suitable pore-widening times for multi-layer substrates.

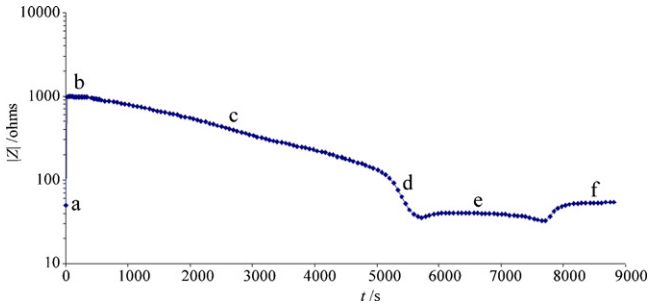

Fig. 8. Impedance magnitude, $|Z|$, at 300 Hz during pore-widening of 2.0 cm^2 of pure aluminium coverslip in 4% phosphoric acid at 21 °C: (a) the initial aluminium substrate with $|Z| = 50\ \Omega$; (b) anodisation increases $|Z|$ to ~990 Ω. Anodisation was stopped after 328 s leaving un-anodised aluminium and titanium below the porous film; (c) the unbiased pore-widening etch results in a decrease in impedance as the barrier oxide and pore walls are thinned; (d) the porous layer is eventually completely etched leaving a planar aluminium surface with impedance ~40 Ω, similar to the initial surface; (e) the remaining aluminium is thinned; and (f) the titanium layer is eventually reached and results a slightly higher impedance of ~53 Ω, probably due to its slenderness of only ~40 nm.

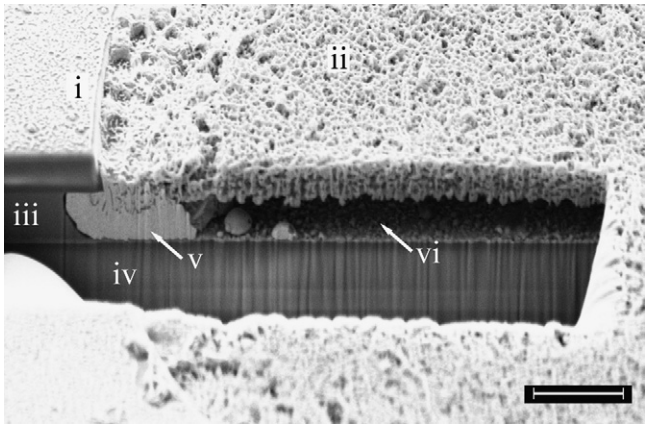

Fig. 9. Platinum deposition of an anodised IC pad: SEM image taken at 36° after FIB cross-sectioning. The circular edge of the pad is shown at (i) and porous alumina electrode surface (ii). The aluminium track leaving the pad is at (iii) which connects to the bondpads at the edge of the IC. The insulating interlayer (iv) dielectric is below the metallisation, with silicon substrate below but out of view. The P-salt bath resulted in poor deposition, generally plating only at the pad periphery (v), and caused dissolution of the alumina film from it base upwards (vi). Scale bar is 2 μm (calibrated for cross-section only).

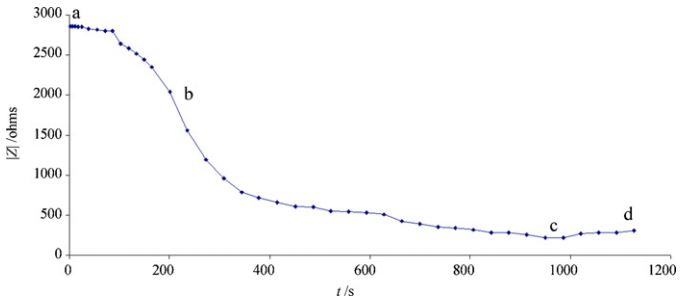

Fig. 10. Impedance magnitude, $|Z|$, versus time, t, for gold deposition into pores of an Al–Si–Cu coverslip of area 1.0 cm^2: (a) nucleation; (b) pores filling; (c) a minimum impedance is reach as the gold emerges with high roughness, i.e. creating an effective surface area larger than the geometric (planar) area; and (d) the impedance increases as the gold roughness decreases and forms a more planar surface.

is believed that the slow plating was caused by a very low current efficiency when operated below ~85 °C [18]. SEM/FIB analysis showed little platinum and dissolution of the alumina at the pore bases, eroding the porous structure upwards towards its surface (Fig. 9). This, combined with the observed gas evolution, suggests hydrogen evolution may have dominated platinum deposition at the barrier oxide or titanium layer, possibly causing a localised low pH due to the higher H^+ ion concentration. This is also supported by the fact that current efficiency for P-salt at 35 °C is known to be low [18]. It was postulated that a factor in the poor deposition

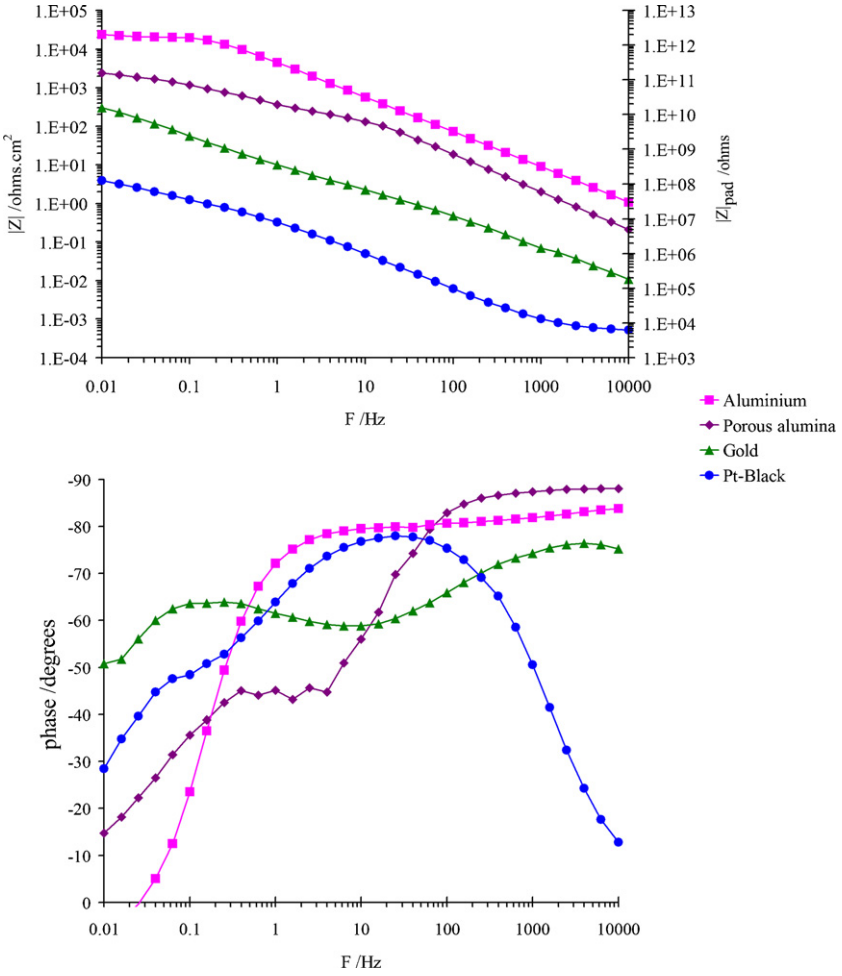

Fig. 11. Impedance magnitude, $|Z|$, per unit area and phase, ϕ, for an IC array at various stages of processing: unprocessed CMOS pads ('aluminium'); after anodising and electrochemical thinning ('porous alumina'); after gold deposition into the pores ('gold'); and after platinum-black deposition ('Pt-black'). Data are for a 48-electrode array, each electrode being 30 μm diameter. The individual electrode impedance, $|Z|_{pad}$, is shown on the second y-axis for reference.

may have been the remaining oxide barrier. The following process modifications were investigated: using partially anodised coverslips (see definition in Section 2.6) to provide a lower impedance substrate; extending voltage ramp thinning to 0.5 V instead of 5.0 V; performing a 'full' anodisation followed by a pore-widening etch; oxalic-based anodisation instead of phosphoric. None of these factors improved deposition using the P-salt.

These problems were overcome by replacing the platinum by a gold chloride bath which had higher metal concentration and higher current efficiency at room temperature [18,28]. The $|Z|$–t plot of Fig. 10 shows the various stages of deposition into porous alumina and is in agreement with the I–t characteristic discussed in ref. [13].

Having achieved the goal of deposition of a noble metal into the porous alumina, the +70 mA/−3 V PED scheme was revisited to determine if it could be simplified. The circuit was replaced by a simple positive pulse (100 ms period, 10–50% duty) generated directly by a waveform generator (Agilent 33220A). This produced results indistinguishable from those achieved with the +70 mA/−3 V circuit. It is therefore likely that, for our thin 1 μm substrates, the simplified PED scheme is acceptable due to the lower aspect ratio of the porous alumina compared to the porous films of up to 50 μm used by others [16,29,30]. Similar, and simpler schemes such as a.c. and d.c. bias, have been successfully used elsewhere to deposit metals into porous alumina films [13,31].

The commercial gold cyanide bath was evaluated as a comparison to the gold chloride bath. Deposition with cyanide was non-uniform with an appearance similar to ICs processed using the P-salt. The cause of this difference is not yet understood, but it is noted that the cyanide (pH ~5) and P-salt (pH 7) baths were less acidic than the gold chloride (pH 0.5). This warrants further investigation. Platinum-black was deposited on electrodes produced using the gold chloride bath to reduce further the impedance.

Fig. 11 shows impedance magnitude, $|Z|$, per unit area and phase, ϕ, for IC arrays. Unprocessed CMOS pads showed a predominantly capacitive characteristic (i.e. $\phi < -70^\circ$ except at low frequencies) which is due to the double layer capacitance [2]. This is usually considered a 'constant phase element' due to the phase being somewhat larger than -90°. Each processing step resulted in a reduction of impedance — anodising and electrochemically thinning, gold deposition and platinum-black. The phase indicates the electrode characteristics become less dominated by the double layer capacitance during processing, with the platinum-black showing more significant resistive elements: at high frequencies the impedance magnitude of the double layer becomes sufficiently low to allow the solution resistance to start to dominate the system, as illustrated by the reduced magnitude of $d|Z|/df$ and the increased phase angle. Fitting these elements to an equivalent circuit is discussed in ref. [10] and is expected to be useful for future amplifier design work.

These completed electrodes (Fig. 12) therefore present biocompatible surfaces with lower impedances than the unmodified aluminium and have similar electrical performance of microelectrodes produced by others [10,32]. Depositing platinum-black using the chloroplatinic acid bath reduced the impedance of the gold pads by a factor (at 1 kHz) of at least 50 (and often by a factor of up to 250), making the electrode more suitable for neuronal recording applications.

3.6. Application suitability

The basic porous alumina CMOS electrode with thinned barrier oxide provides functional biocompatible electrodes suited to many biological applications such as cell-substrate impedance sensing [32] and manipulation of cells and proteins by ((negative-)di-)electrophoresis [33]. However, it is possible that the lateral linking of adjacent pores seen in the CMOS metallisation may prevent the plain porous alumina electrode from successfully recording action potentials from adherent neurons. For this particular application, or others requiring a non-porous surface, we have shown that the pores can be filled with a bio-inert noble metal. This retains

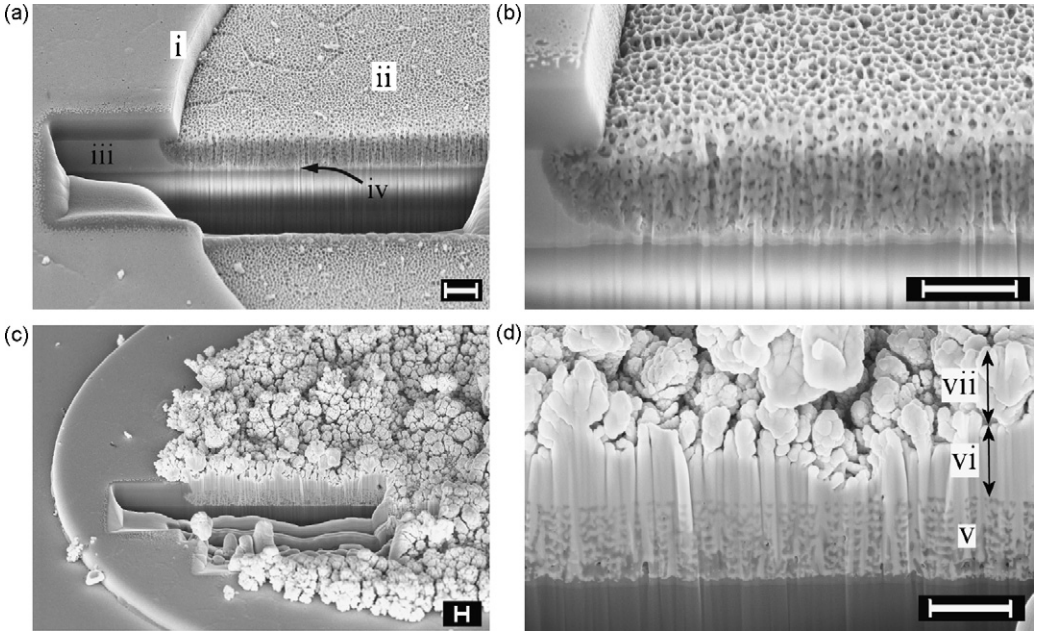

Fig. 12. Completed biocompatible electrodes (SEM images using the 'In-lens' detector, taken at 36° after FIB cross-sectioning): (a) porous alumina electrode with a FIB section, showing the circular edge (i) of the electrode and porous surface (ii); the aluminium track (iii) is electrically connected to the titanium layer (iv); (b) higher magnification of the same electrode showing the branching alumina pores and thin titanium layer; (c) porous alumina and gold electrode enhanced with platinum-black for lower impedance; and (d) high magnification of the FIB section in (c) showing the pores (v) filled with gold. At the top of the porous layer the gold deposition has been allowed to continue so to form a solid film (vi) that fills the pad opening up to the chip surface. The high surface area of the subsequent platinum-black deposition (vii) can be seen along the top of the image. A distinct interface between the gold and platinum-black cannot be seen in the image (60 V phosphoric anodisation to cusp; exponential ramp to 5 V; gold chloride deposition; platinum-black duration to achieve ≤40 kΩ per electrode). Scale bars are 1 μm.

the benefit of removing the electrochemically active aluminium from the vicinity of cells and culture medium without the need to modify the CMOS using non-standard and costly clean room facilities. Low noise electrodes for small signal neuronal recordings require minimising the impedance and this is likely to require the platinum-black deposition.

4. Conclusion

It has been demonstrated that CMOS microelectrodes can be made biocompatible by removing corrosive aluminium by converting it to nanoporous aluminium oxide. This was achieved through anodisation and barrier oxide thinning, resulting in an impedance comparable to the unmodified aluminium and other planar electrodes. The manufacturing scheme also tailors the impedance and porosity of films by thinning the barrier oxide and widening the pores. Infiltrating pores with metal further reduces impedance. For applications requiring a planar electrode surface, gold was electrodeposited into the porous alumina to provide a bio-inert surface. For neuronal recording applications that often call for particularly low impedances, the planar gold electrode was coated with platinum-black resulting in at least a further 50-fold reduction in impedance.

The work was made possible by real-time impedance spectroscopy during anodisation, electrochemical thinning, pore-widening and electrodeposition processes, and can be used as a flexible tool for the study of many electrochemical systems.

FIB was used to produce cross-sectional cuts to study the IC anodisation and electroplating processes. The SEM "In-lens" detector provided high-resolution images and gave a unique morphological contrast which further assisted analysis.

This low-cost process has been developed for manufacturability and enables CMOS integrated circuits, fabricated using standard processing, to be used as biocompatible microelectrodes.

Acknowledgements

This work has been funded by the UK Engineering and Physical Sciences Research Council (EPSRC) via a doctoral training grant, EPSRC 'Access to Nanoscience and Nanotechnology Equipment' (EP/F056745/1) and the University of Bath Enterprise Development Fund.

Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at doi:10.1016/j.snb.2010.03.030.

References

[1] J.J. Pancrazio, J.P. Whelan, D.A. Borkholder, W. Ma, D.A. Stenger, Development and application of cell-based biosensors, Ann. Biomed. Eng. 27 (1999) 697–711.
[2] A.H.D. Graham, C.R. Bowen, J. Robbins, J. Taylor, Formation of a porous alumina electrode as a low-cost CMOS neuronal interface, Sens. Actuator B-Chem. 138 (2009) 296–303.
[3] A.H.D. Graham, C.R. Bowen, J. Taylor, J. Robbins, Neuronal cell biocompatibility and adhesion to modified CMOS electrodes, Biomed. Microdevices 11 (2009) 1091–1101.
[4] G.D. Sulka, W.J. Stepniowski, Structural features of self-organized nanopore arrays formed by anodization of aluminum in oxalic acid at relatively high temperatures, Electrochim. Acta 54 (2009) 3683–3691.
[5] S.-K. Hwang, S.-H. Jeong, H.-Y. Hwang, O.-J. Lee, K.-H. Lee, Fabrication of highly ordered pore array in anodic aluminum oxide, Korean J. Chem. Eng. 19 (2002) 467–473.
[6] S. Ono, M. Saito, M. Ishiguro, H. Asoh, Controlling factor of self-ordering of anodic porous alumina, J. Electrochem. Soc. 151 (2004) B473–B478.
[7] W. Chen, J.-S. Wu, X.-H. Xia, Porous anodic alumina with continuously manipulated pore/cell size, ACS Nano 2 (2008) 959–965.
[8] M.D. Abramoff, P.J. Magelhaes, S.J. Ram, Image processing with ImageJ, Biophoton. Int. 11 (2004) 36–42.
[9] G.D. Sulka, V. Moshchalkov, G. Borghs, J.-P. Celis, Electrochemical impedance spectroscopic study of barrier layer thinning in nanostructured aluminium, J. Appl. Electrochem. 37 (2007) 789–797.
[10] W. Franks, I. Schenker, P. Schmutz, A. Hierlemann, Impedance characterization and modeling of electrodes for biomedical applications, IEEE Trans. Biomed. Eng. 52 (2005) 1295–1302.
[11] F. Li, L. Zhang, R.M. Metzger, On the growth of highly ordered pores in anodized aluminum oxide, Chem. Mater. 10 (1998) 2470–2480.
[12] J.M. Montero-Moreno, M. Belenguer, M. Sarret, C.M. Muller, Production of alumina templates suitable for electrodeposition of nanostructures using stepped techniques, Electrochim. Acta 54 (2009) 2529–2535.
[13] A. Ghahremaninezhad, A. Dolati, A study on electrochemical growth behavior of the Co–Ni alloy nanowires in anodic aluminum oxide template, J. Alloy. Compd. 480 (2009) 275–278.
[14] A. Saedi, M. Ghorbani, Electrodeposition of Ni–Fe–Co alloy nanowires in modified AAO template, Mater. Chem. Phys. 91 (2005) 417–423.
[15] S.K. Lim, G.H. Jeong, I.S. Park, S.M. Na, S.J. Suh, Fabrication of electrodeposited Co–Pt nano-arrays embedded in an anodic aluminum oxide/Ti/Si substrate, J. Magn. Magn. Mater. 310 (2007) e841–e842.
[16] G.P. Sklar, K. Paramguru, M. Misra, J.C. LaCombe, Pulsed electrodeposition into AAO templates for CVD growth of carbon nanotube arrays, Nanotechnology 16 (2005) 1265–1271.
[17] K. Nielsch, F. Müller, A.-P. Li, U. Gösele, Uniform nickel deposition into ordered alumina pores by pulsed electrodeposition, Adv. Mater. 12 (2000) 582–586.
[18] M.E. Baumgärtner, C.J. Raub, The electrodeposition of platinum and platinum alloys, Platinum Met. Rev. 32 (1988) 188–197.
[19] X. Zhou, G.E. Thompson, H. Habazaki, K. Shimizu, P. Skeldon, G.C. Wood, Copper enrichment in Al–Cu alloys due to electropolishing and anodic oxidation, Thin Solid Films 293 (1997) 327–332.
[20] M.A. Paez, O. Bustos, G.E. Thompson, P. Skeldon, K. Shimizu, G.C. Wood, Porous anodic film formation on an Al–3.5 wt% Cu alloy, J. Electrochem. Soc. 147 (2000) 1015–1020.
[21] G.E. Thompson, H. Habazaki, K. Shimizu, M. Sakairi, P. Skeldon, X. Zhou, G.C. Wood, Anodizing of aluminium alloys, Aircr. Eng. Aerosp. Technol. 71 (1999) 228–238.
[22] H. Habazaki, K. Shimizu, M.A. Paez, P. Skeldon, G.E. Thompson, G.C. Wood, X. Xhou, Oxidation of copper and mobility of copper ions during anodizing of an Al–1.5 wt% Cu alloy, Surf. Interface Anal. 23 (1995) 892–898.
[23] A.J. Griffin Jr., F.R. Brotzen, C.F. Dunn, Impedance-spectroscopy response of aluminum-copper-silicon alloys, J. Electrochem. Soc. 141 (1994) 3473–3479.
[24] E. Palibroda, A. Lupsan, S. Pruneanu, M. Savos, Aluminium porous oxide growth. On the electric conductivity of the barrier layer, Thin Solid Films 256 (1995) 101–105.
[25] S. Wernick, R. Pinner, The Surface Treatment and Finishing of Aluminium and its Alloys, vol.1, 4th ed., Draper, Teddington, UK, 1971.
[26] D. Crouse, Y. Lo, A.E. Miller, M. Crouse, Self-ordered pore structure of anodized aluminum on silicon and pattern transfer, Appl. Phys. Lett. 76 (2000) 49–51.
[27] G.E. Thompson, Porous anodic alumina: fabrication, characterization and applications, Thin Solid Films 297 (1997) 192–201.
[28] Y. Okinaka, C. Wolowodiuk, Cyanoaurate(III) formation and its effect on current efficiency in gold plating, J. Electrochem. Soc. 128 (1981) 288–294.
[29] O. Rabin, P.R. Herz, Y.-M. Lin, A.I. Akinwande, S.B. Cronin, M.S. Dresselhaus, Formation of thick porous anodic alumina films and nanowire arrays on silicon wafers and glass, Adv. Funct. Mater. 13 (2003) 631–638.
[30] H. Mori, T. Korenaga, N. Hosomi, T. Terui, S. Shingubara, Filling of FePt in AAO nanohole array by DC pulsed electrodeposition, Electrochem. Soc. Trans. 16 (45) (2009) 65–71.
[31] M.T. Wu, I.C. Leu, J.H. Yen, M.H. Hon, Preparation of Ni nanodot and nanowire arrays using porous alumina on silicon as a template without a conductive interlayer, Electrochem. Solid State Lett. 7 (2004) C61–C63.
[32] S.B. Prakash, P. Abshire, A CMOS capacitance sensor that monitors cell viability, IEEE Sens. J. 1–2 (2005) 1177–1180.
[33] N. Mittal, A. Rosenthal, J. Voldman, nDEP microwells for single-cell patterning in physiological media, Lab Chip 7 (2007) 1146–1153.

Biographies

Anthony H.D. Graham received the BEng degree (1988) in Electrical and Electronic Engineering from The University of Nottingham. He then spent 13 years with Intel Corporation as their European memory components quality and reliability engineer and as a corporate quality programs manager. He became partner in a conservation business after receiving an MSc in the Conservation of Historic Buildings from the University of Bath (2004). In 2007 he returned to the University of Bath to undertake a PhD in the Department of Electronic and Electrical Engineering where his interests are extracellular recording of neuronal cells using CMOS integrated circuits.

Chris R. Bowen is a Reader in materials at the Department of Mechanical Engineering, University of Bath. He obtained a DPhil from the University of Oxford on the thermal modelling and processing of ceramic composites. He undertook postdoctoral research at the Technical University of Hamburg-Harburg on ceramic composites and was a Senior Scientist at Defence Evaluation and Research Agency. His current research areas include electromechanical properties of functional materials and composites, dielectric materials and polarised biomaterials. He has over 90

papers in refereed journals and is a member of the UK Smart Materials and Systems Committee of the Institute of Materials.

Jon Robbins received a BSc in Physiology from University College London in 1982 and a PhD in Neurophysiology from the University of London (UMDS) in 1987. At King's College London he became a Fellow of the Higher Education Academy in Teaching Practice (2002) and is a Senior Lecturer in Pharmacology, the Senior Tutor in Neuroscience and an Honorary Lecturer in Pharmacology at University College London. His research interests are the role and modulation of ion channels in neuronal cells and he has published over 100 papers, book chapters and conference proceedings.

Georgi Lalev leads the Nano-manufacturing Technologies Lab, which is part of the Manufacturing Engineering Centre (MEC) at Cardiff University. He obtained his PhD in Engineering from Tohoku University, Japan, investigating the epitaxial growth of II–VI semiconductors. His primary task in the Centre is to develop and validate novel cost effective manufacturing routes for 2.5D and 3D nano/micro structuring. His expertise is in nano-manufacturing and particularly in UV-nanoimprinting, focused ion beam machining and inspection.

Frank Marken is a Reader in physical chemistry at the Department of Chemistry, University of Bath. He obtained a Dr. rer. nat. degree from the RWTH, Aachen. He has specialised in the field of electrochemistry. Current research focuses on mesoporous films, ion transfer, microwave effects, and novel sensing processes and mechanisms at electrodes.

John Taylor was born at Wanstead, Essex, UK, in 1952 and received the PhD degree from Imperial College, London University, UK, in 1984. He joined the Department of Electronic and Electrical Engineering at the University of Bath in 2002 where he holds the position of Professor of Microelectronics and Optoelectronics. His research interests are in the fields of analogue and mixed analogue/digital system design, including communication systems and implantable devices for biomedical applications. Professor Taylor has published more than 150 technical papers in international journals and conferences and has co-edited a handbook on filter design.